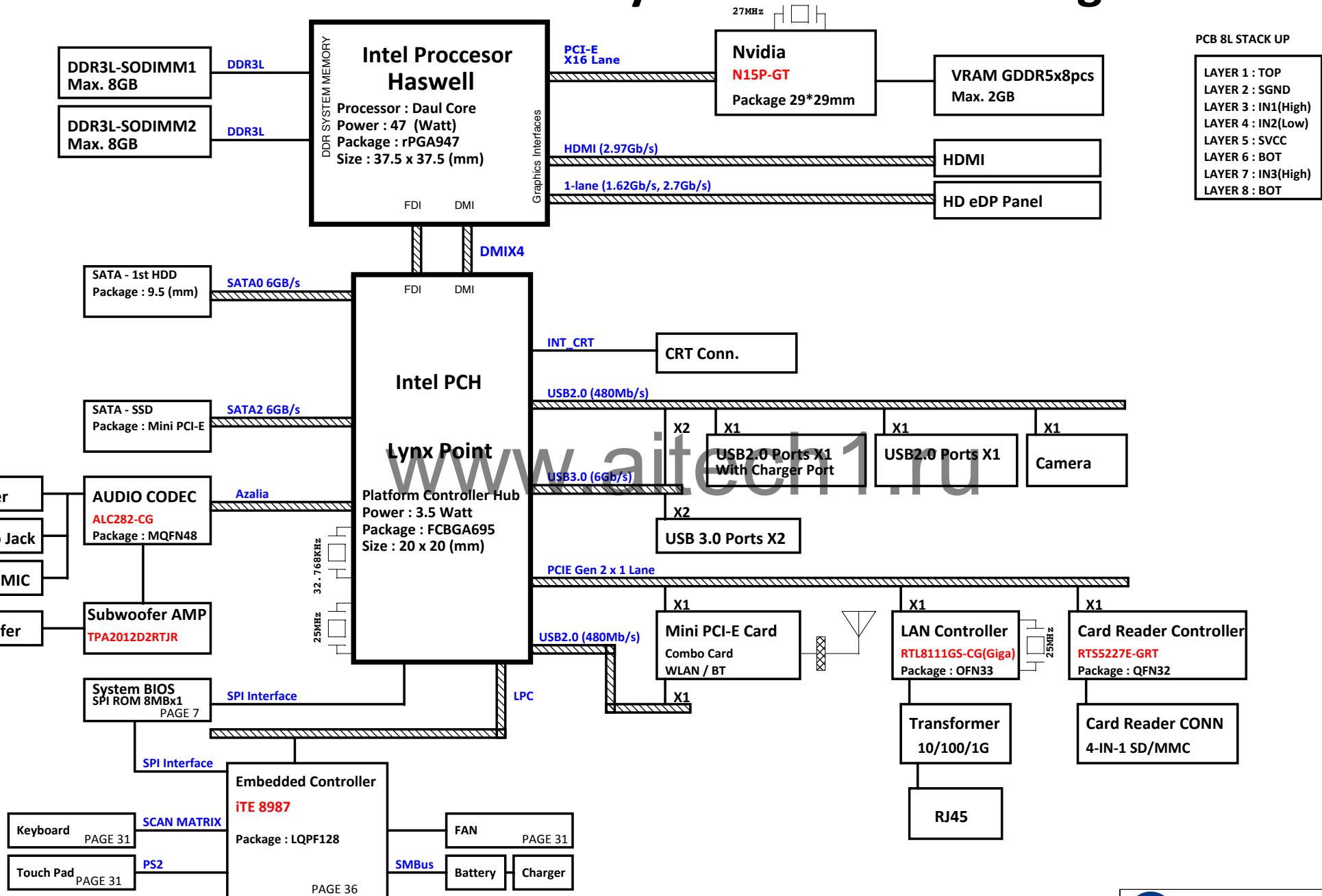
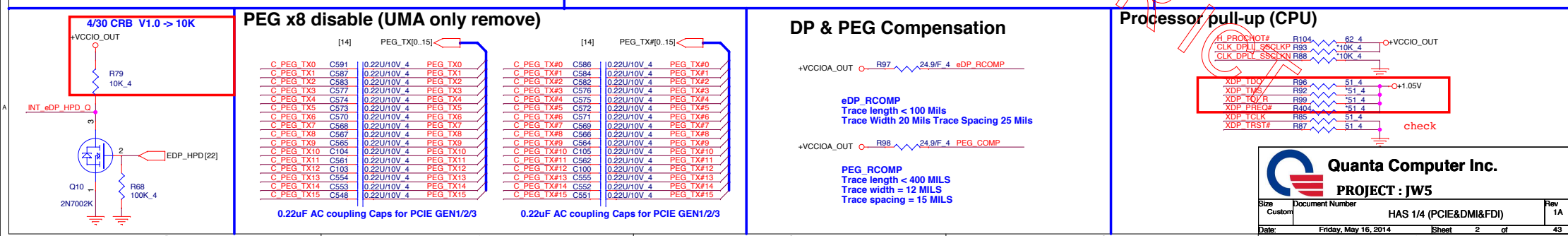
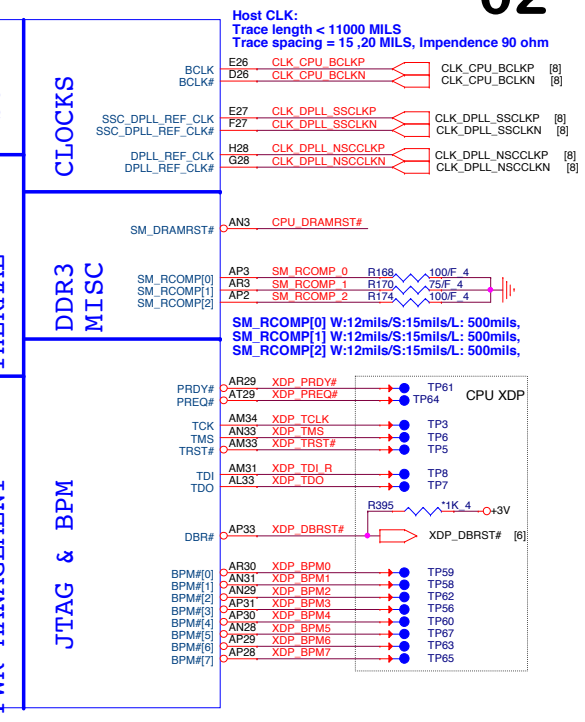


JW5 Intel Shark Bay Platform Block Diagram

01

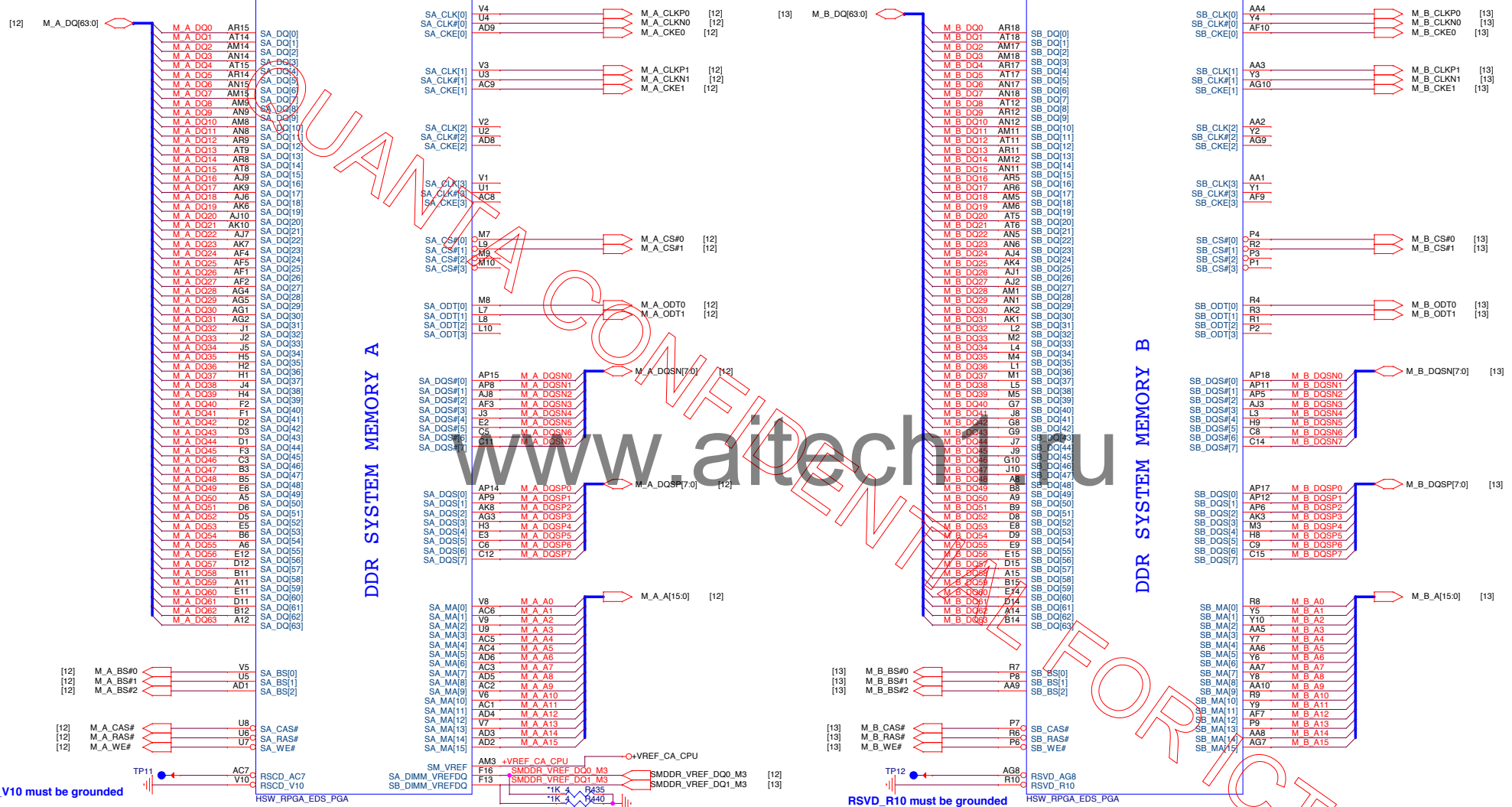




Haswell Processor (DDR3)

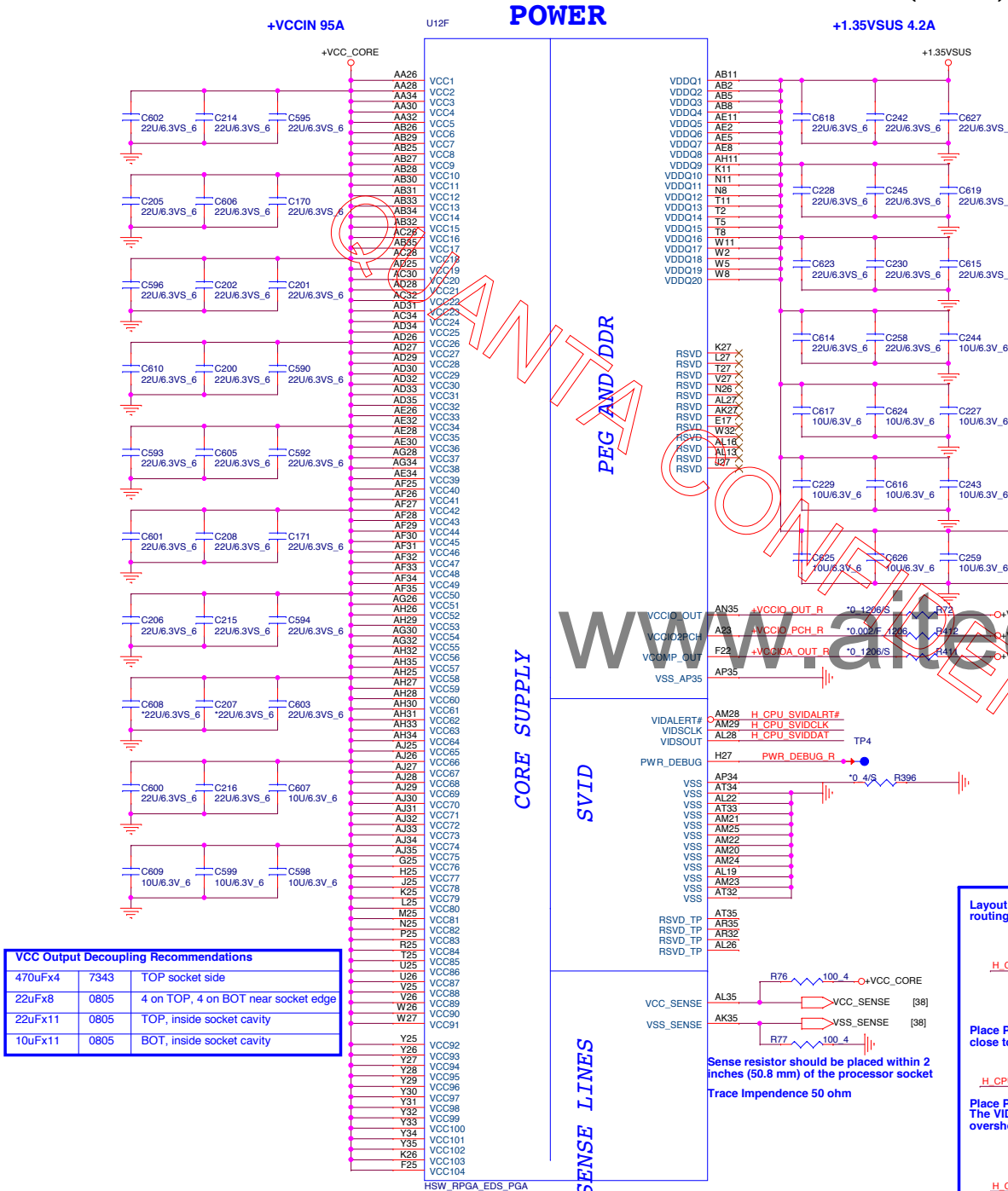
U12C

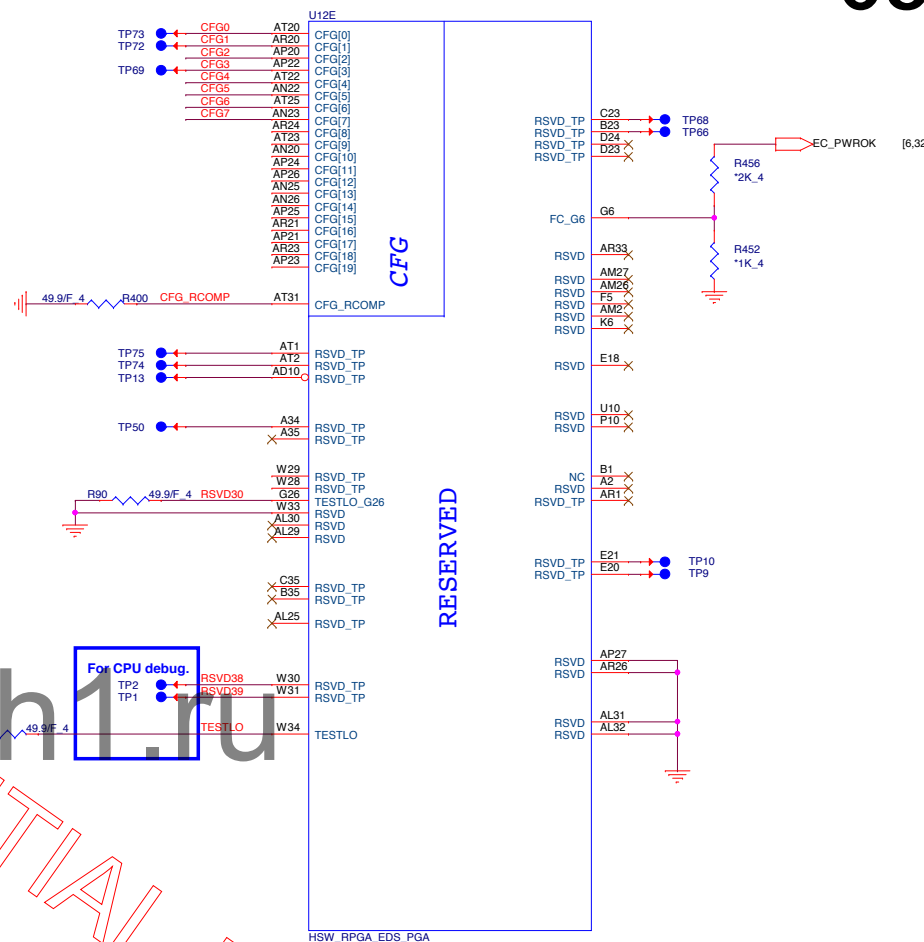
U12D



Haswell Processor (POWER)

04

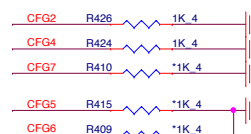




CFG3 R413 *1K_4

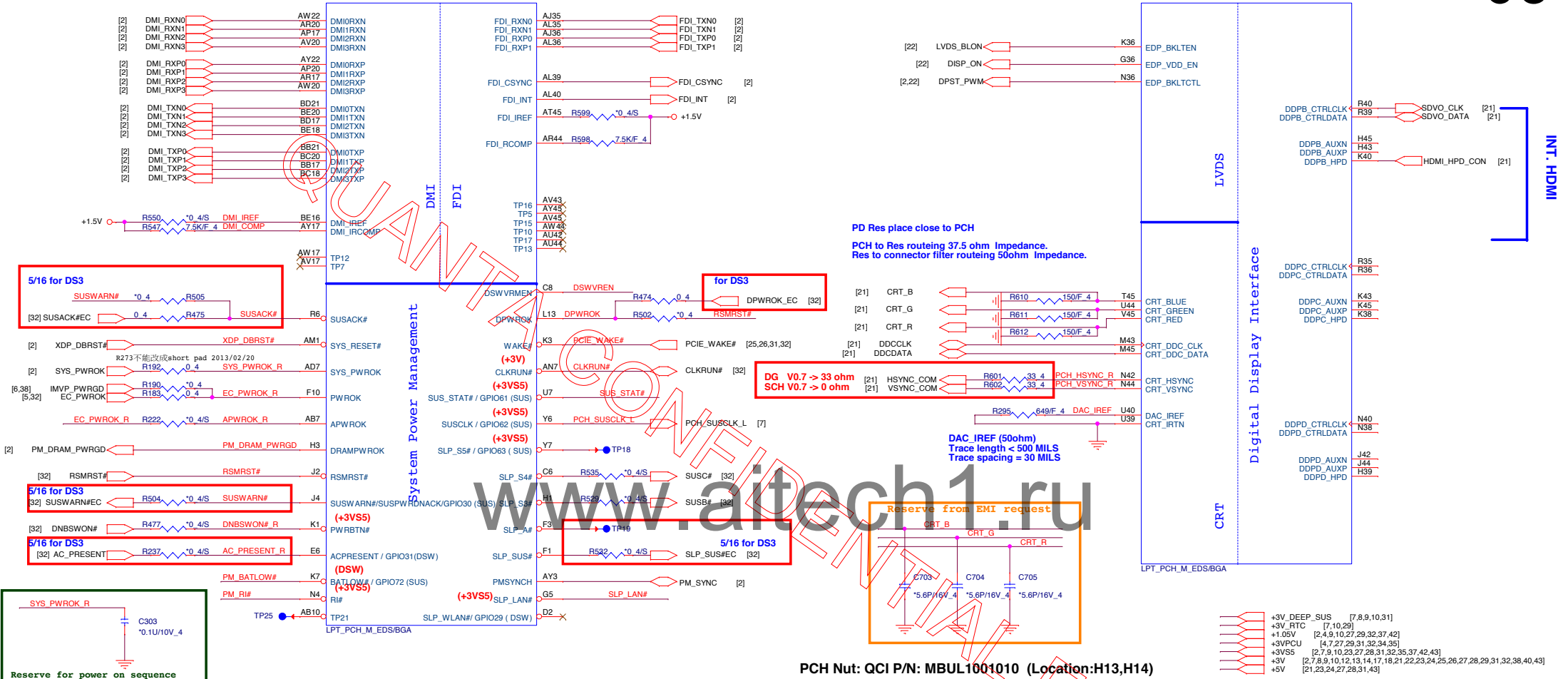
```
11: (Default) x16 - Device 1 functions 1 and 2 disabled
10: x8, x8 - Device 1 function 1 enabled ; function 2 disabled
01: Reserved - (Device 1 function 1 disabled ; function 2 enabled)
00: x8.x4.x4 - Device 1 functions 1 and 2 enabled
```

	1	0
CFG2 (PEG Static Lane Reverse)	Normal Operation	Lane Reversed
CFG4 (DP Presence Strap)	Disable; No physical DP attached to eDP	Enable; An ext DP device is connected to eDP
CFG7 (PEG Defer Training)	PEG train immediately following xxRESETB de assertion	PEG wait for BIOS training

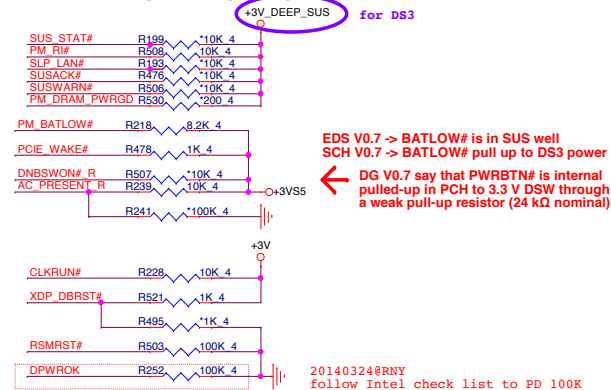


U19C

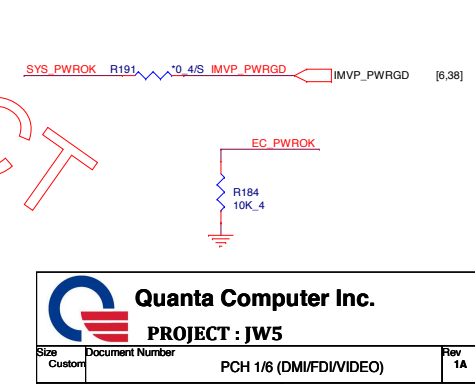
U19D



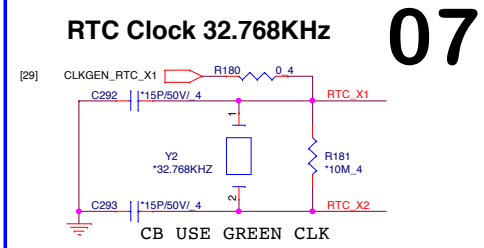
PCH Pull-high/low(CLG)



System PWR_OK(CLG)



07



Port 1 Disable

Port 3 Disable

RTC Power trace width 20mils.

AY5 ~~SATA_RCOMP~~ R233

SATA_RCOMP
Impedance = 50 ohm
Trace length < 500 mils
Trace spacing = 15 mils

The diagram shows a signal line labeled "BIT_CLK_AUDIO" in red. A capacitor, labeled "C693" and "*33P/50V_4", is connected in parallel to ground. The text "EMI" is placed near the capacitor, indicating its function in filtering electromagnetic interference.

PCH JTAG Debug(CLG)

PCH Strap Table

[illegible]

TP81 PCH_SPI_CS0#_R
PCH_SPI_CLK_R

TP63	BIOS WP#
TP76	HOLD#
TP79	

Signal	Value	Unit
PCH_SPI_CS0#	33.4	ns
PCH_SPI1_CLK	33.4	ns

R457/R453/R450/R451/R546/R548 close to U15 pin

Schematic diagram of the +3VSP_I02 power plane. The circuit includes a power source connected to a network of capacitors (C670, 1U/10V_4, 3.3K/F_4, 15/F_4) and resistors (R465, R460) leading to the BIOS component.

[32]	PCH_SPI_CS0#_R	PCH_SPI_CS0#_R
[32]	PCH_SPI1_CLK_R	PCH_SPI1_CLK_R
[32]	PCH_SPI1_SI_R	PCH_SPI1_SI_R

Size	Document Number
Custom	

PCH SPI1 CLK R	6	CE#	VDD
PCH SPI1 SI R	5	SCK	
PCH SPI1 SO R	2	SI	7 HOLD#

PCON ST#	2	SO	HOLD#	7	HOLD#
BIOS_WP#	3	WP#	VSS	4	

*SPI SOCKET
DFHS08FS023

91960-0084L-8P-SOCKET

+3VS5 H473 0.4
 +3V DEEP SUS R501 0.4/S

U16

CE# 6
SCK 5
CS 4

7 HOLD# 15/F_4

WP# VSS
GD25B64BSIGR C673

AKE3EGN0Q01 0.1U/10V_4

WP#	PCH_SPI_IO3
-----	-------------

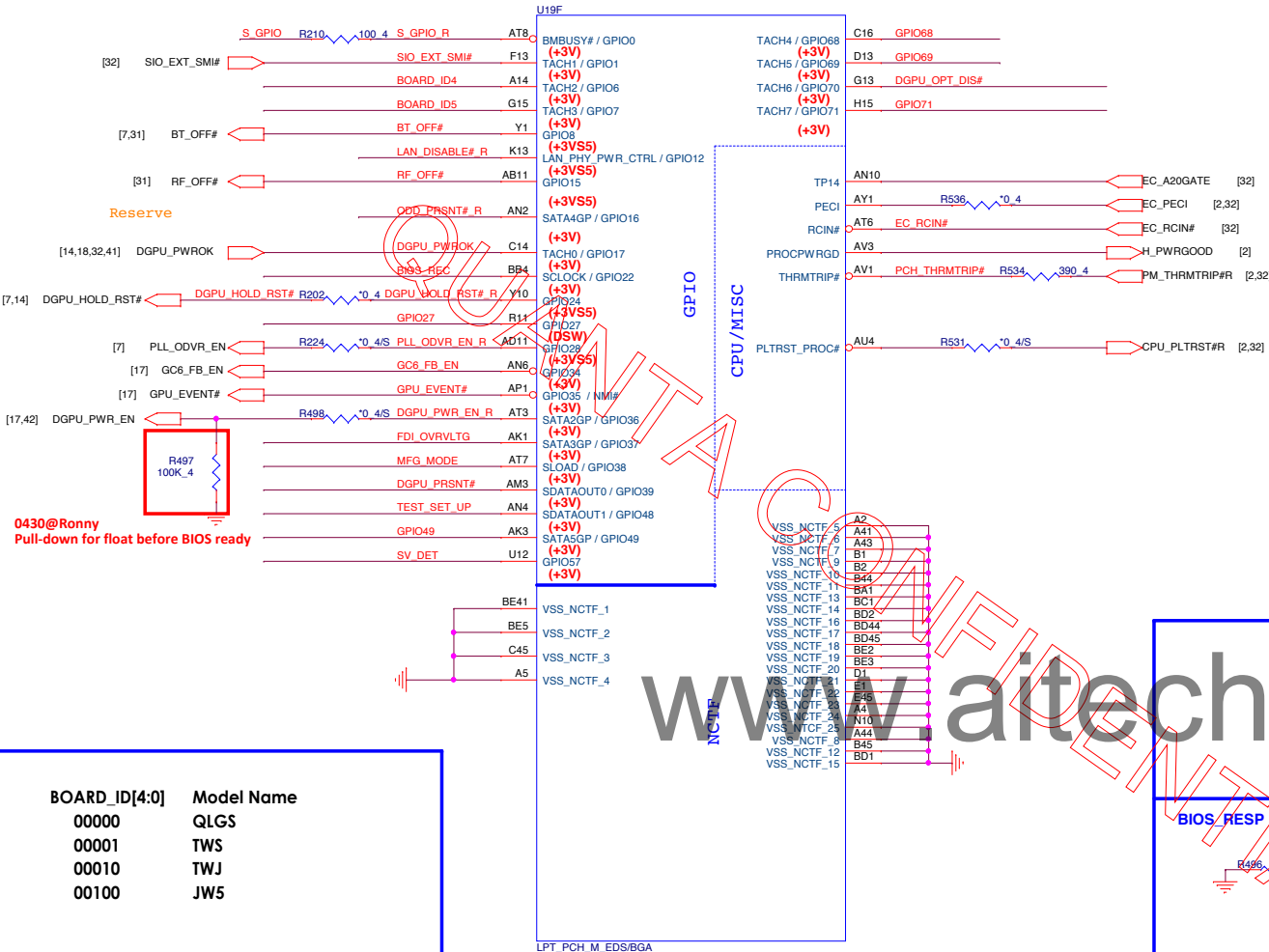
Source: Computer Inc.

Quantia Computer Inc.

PROJECT: JW5

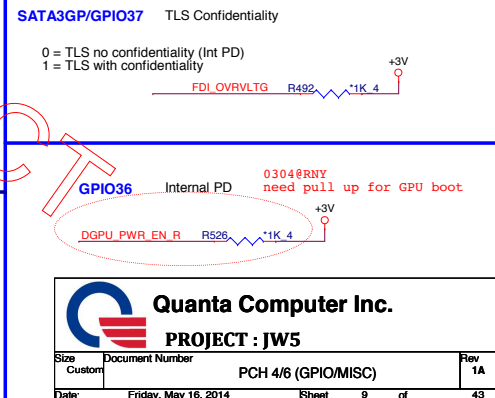
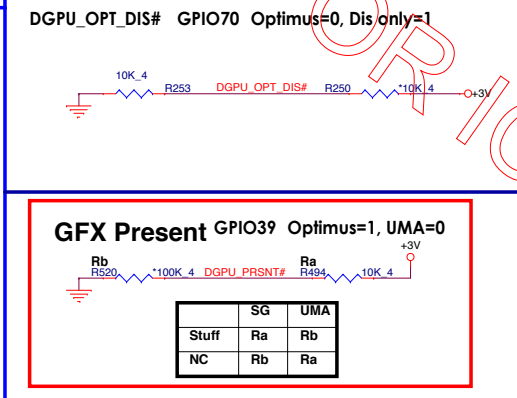
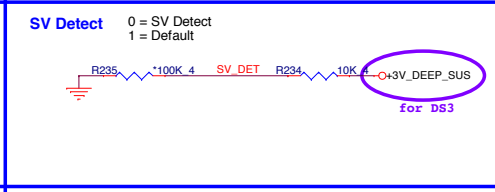
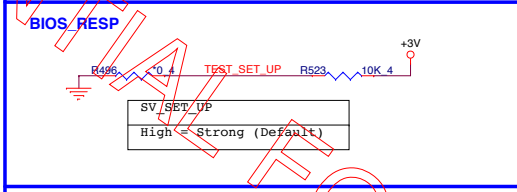
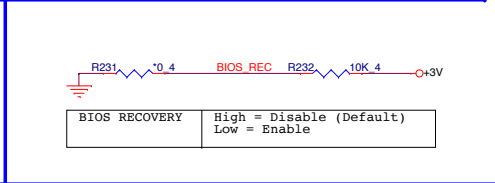
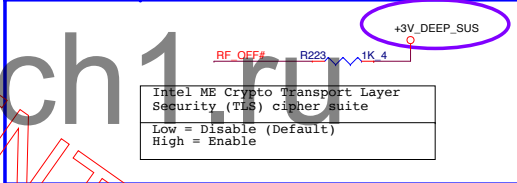
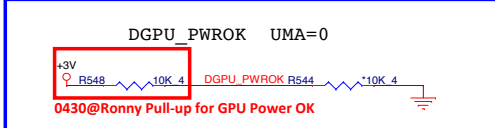
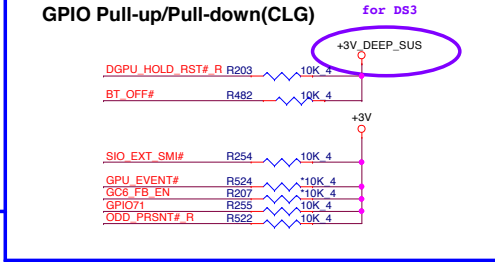
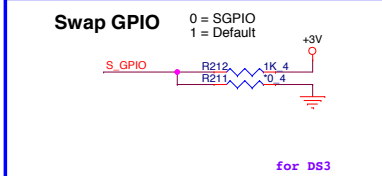
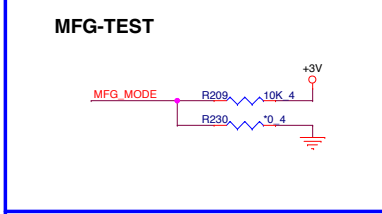
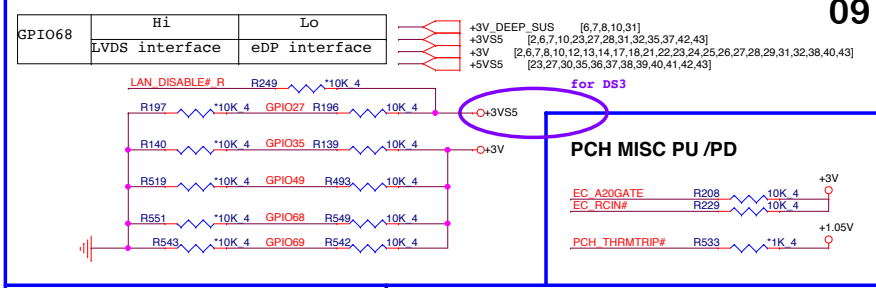
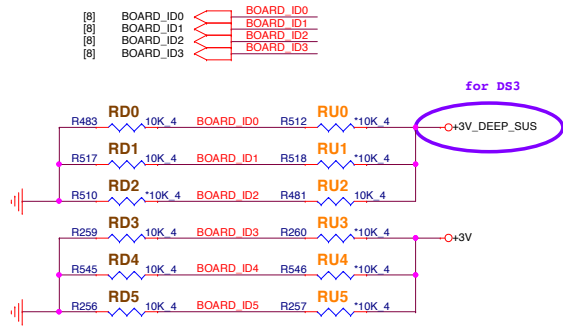
PCH 2/6 (SATA/HDA/SPI)			1A
May 16, 2014	Sheet	7 of	43

Lynx Point (GPIO,VSS_NCTF,RSVD)

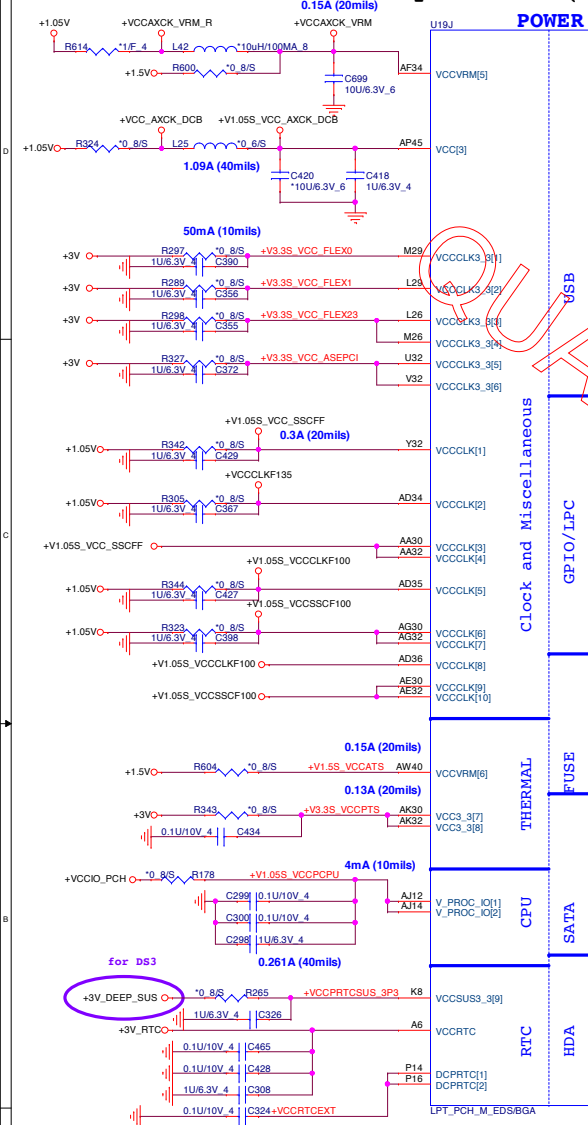


HSW BOARD ID SETTING

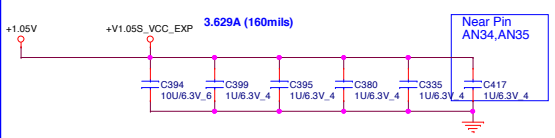
BOARD_ID0	GPIO44	MODEL_BIT0
BOARD_ID1	GPIO45	MODEL_BIT1
BOARD_ID2	GPIO46	MODEL_BIT2
BOARD_ID3	GPIO4	MODEL_BIT3
BOARD_ID4	GPIO6	MODEL_BIT4
BOARD_ID5	GPIO7	No Dolby=0, Dolby=1
GPIO71	GPIO71	Reserve
GPIO35	GPIO35	Reserve
GPIO49	GPIO49	Reserve
GPIO68	GPIO68	Reserve
GPIO69	GPIO69	Reserve
DGPU_PRST	GPIO39	Optimus=1, UMA=0
DGPU_OPT_DIS#	GPIO70	Optimus=0, Dis only=1



Lynx Point (POWER)

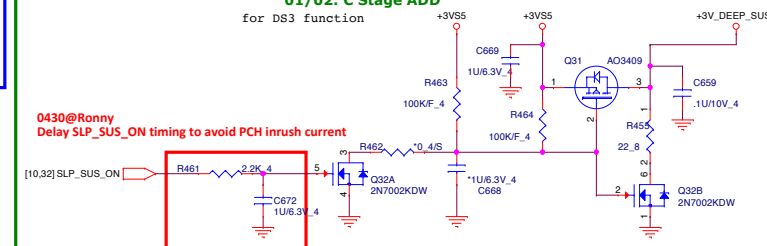


PCH VCCIO Power



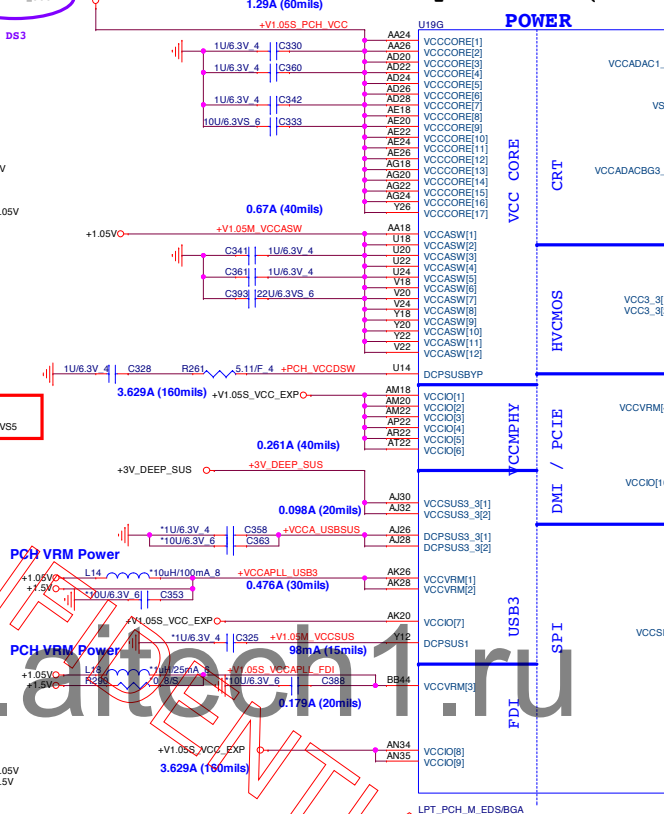
01/02: C S

for DS3 function

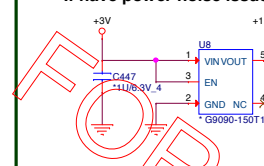


0430@Ronny
Delay SLP_SUS_ON timing to avoid PCH inrush current

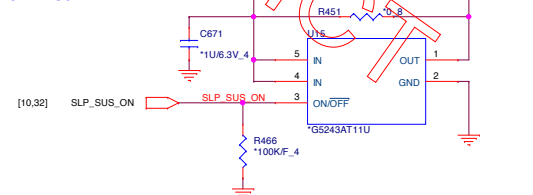
Lynx Point (POWER)



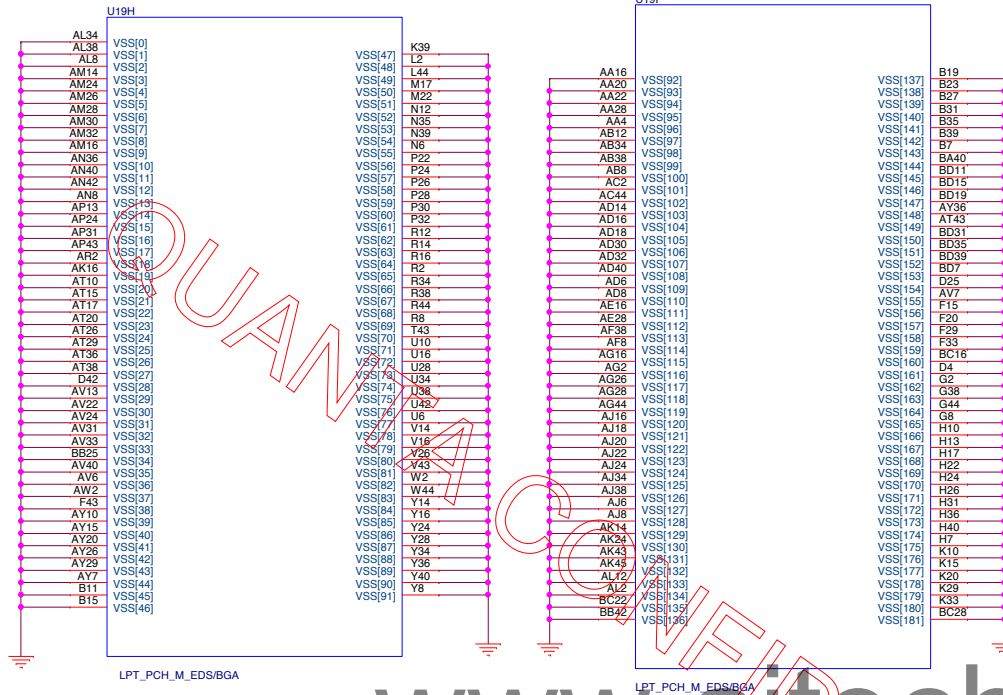
If have power noise issue then stuff it.

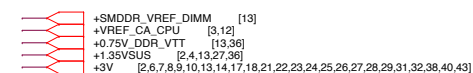


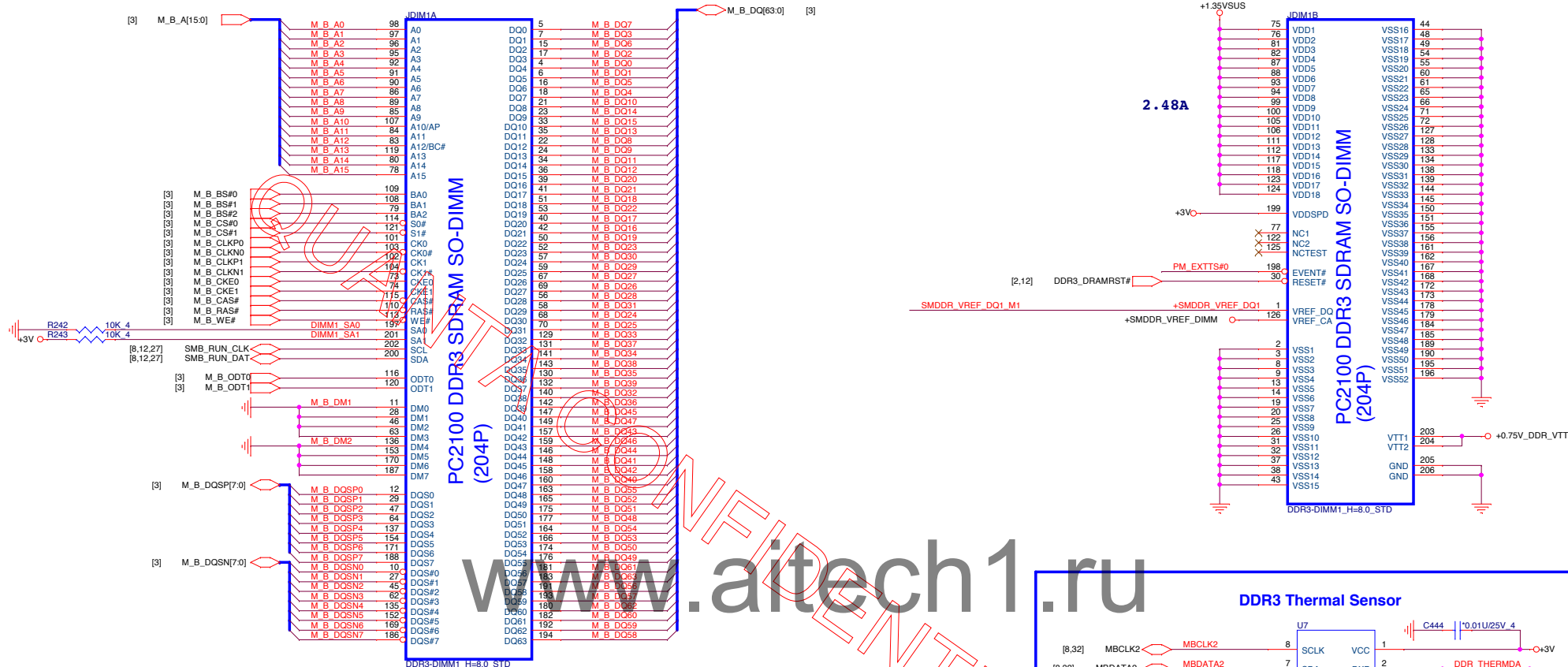
PCH DS3 PWR



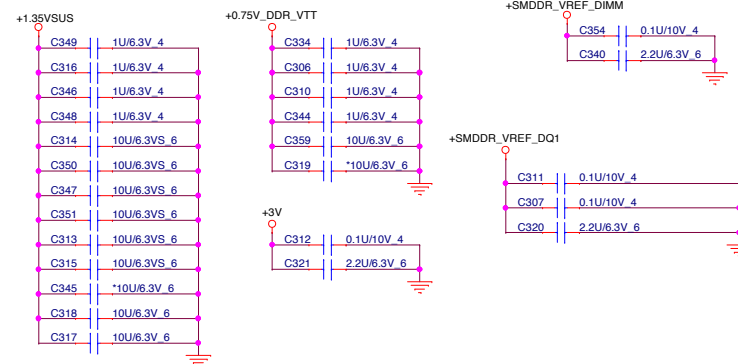
Lynx Point (GND)



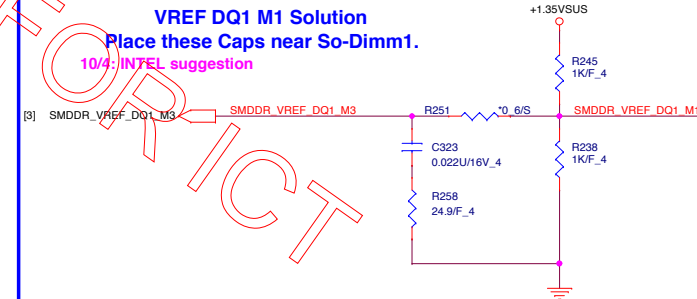


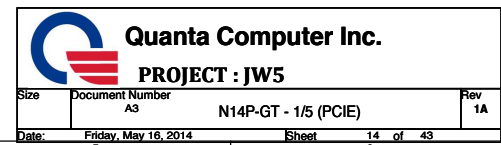


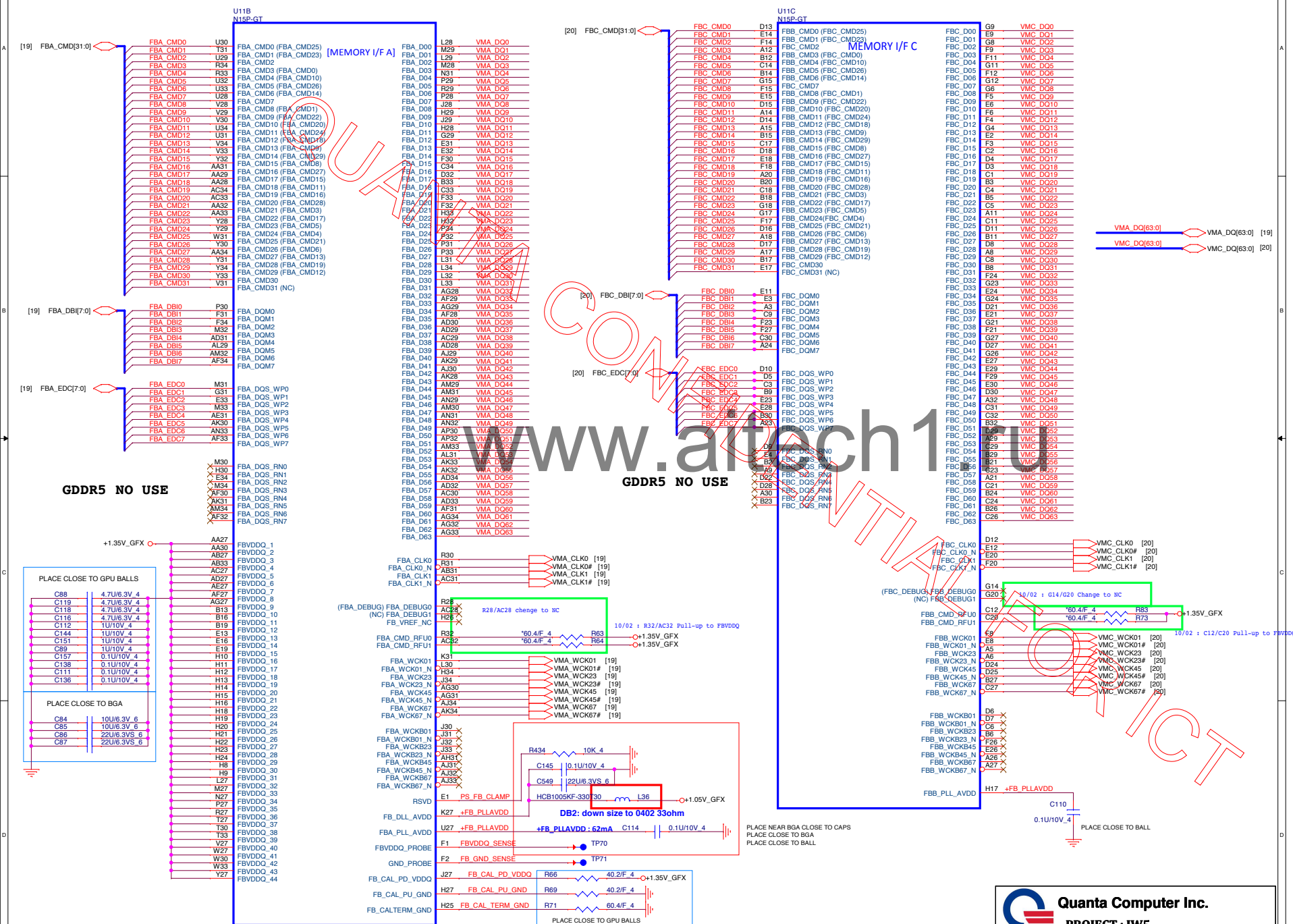
Place these Caps near So-Dimm1.

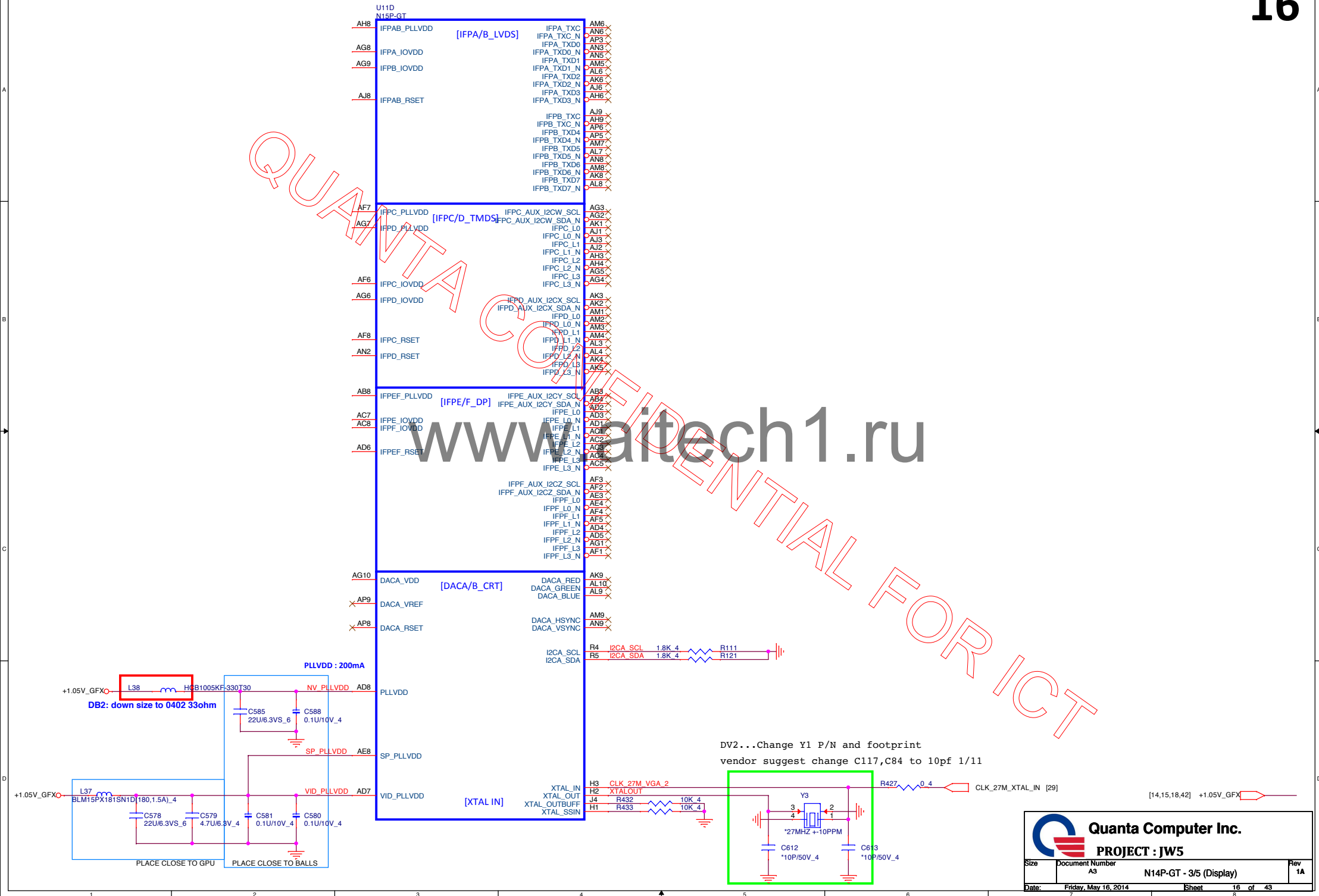


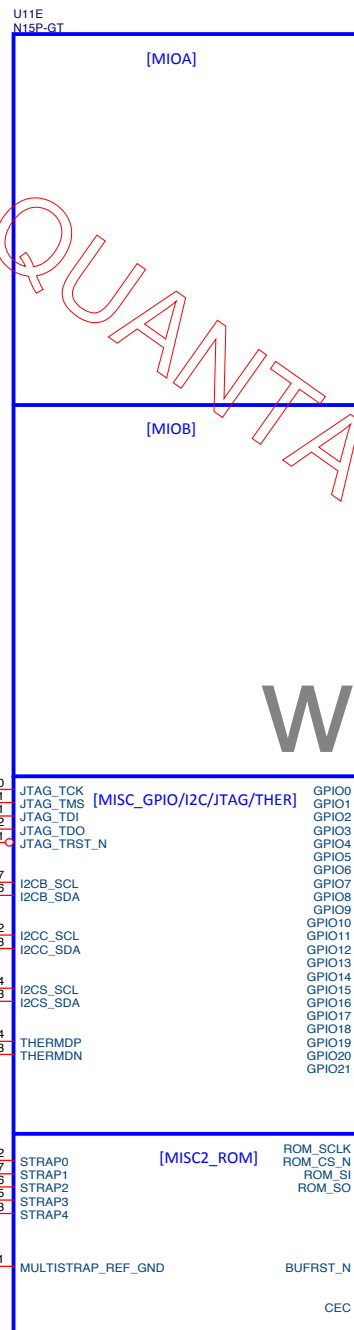
VREF DQ1 M1 Solution
Place these Caps near So-Dimm1.
10/4: INTEL suggestion











	ROM_SI
	ROM_SO
	ROM_SCLK
N15P-GT	by VRAM

Default: N15P-GT Hynix 2G VRAM

Vendor	Q : P/N	Mfr. P/N
Hynix	AKG5MWUTW23	H5GC2H24BFR-T2C
Samsung	AKG5MWDTS02	K4G20325FD-FC03

GPU	VRAM description and P/N	Supplier	Q'ty	VRAM size	Strap	Multistrap_ref_gnd	ROM_SCLK	ROM_SI	ROM_SO	STRAP0	STRAP1	STRAP2	STRAP3	STRAP4
GT850M	IC SGRAM[170P]H5GC2H24BFR-T2C(BGA)	Hynix	8	2G (128x16)	0x1	40.2K PD	4.99K PD	10K PD	4.99K PD	50K PU	NC	NC	NC	NC
N15P-GT-A2(BGA)	P/N:AKG5MWUTW23													
P/N:AJUN15POT00	IC SGRAM[170P]K4G20325FD-FC03 FBGA	Samsung	8	2G (128x16)	0x0	40.2K PD	4.99K PD	4.99K PD	4.99K PD	50K PU	NC	NC	NC	NC
	P/N:AKG5MWDTS02													

4.99K/F 4: CS24992FB26 RES CHIP 4.99K 1/16W +1% (0402)
 10K/F 4: CS31002FB26 RES CHIP 10K 1/16W +1% (0402)
 15K/F 4: CS31502FB29 RES CHIP 15K 1/16W +1% (0402)
 20K/F 4: CS32002FB29 RES CHIP 20K 1/16W +1% (0402)
 24.9K/F 4: CS32492FB16 RES CHIP 24.9K 1/16W +1% (0402)
 30.1K/F 4: CS33012FB18 RES CHIP 30.1K 1/16W +1% (0402)
 34.8K/F 4: CS33482FB22 RES CHIP 34.8K 1/16W +1% (0402)
 45.3K/F 4: CS34532FB18 RES CHIP 45.3K 1/16W +1% (0402)

Logical Strap Bit Mapping

Table 15-2. Resistance Mapping to Hex Values

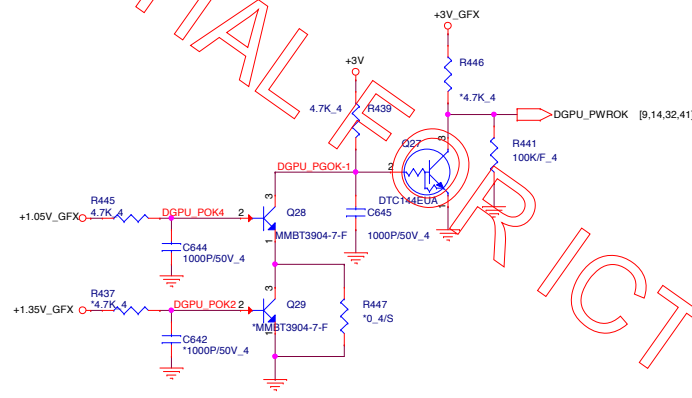
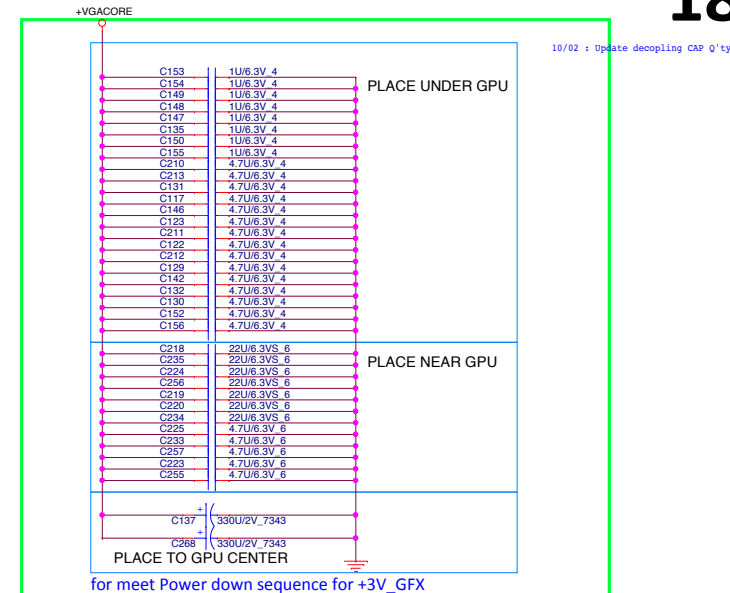
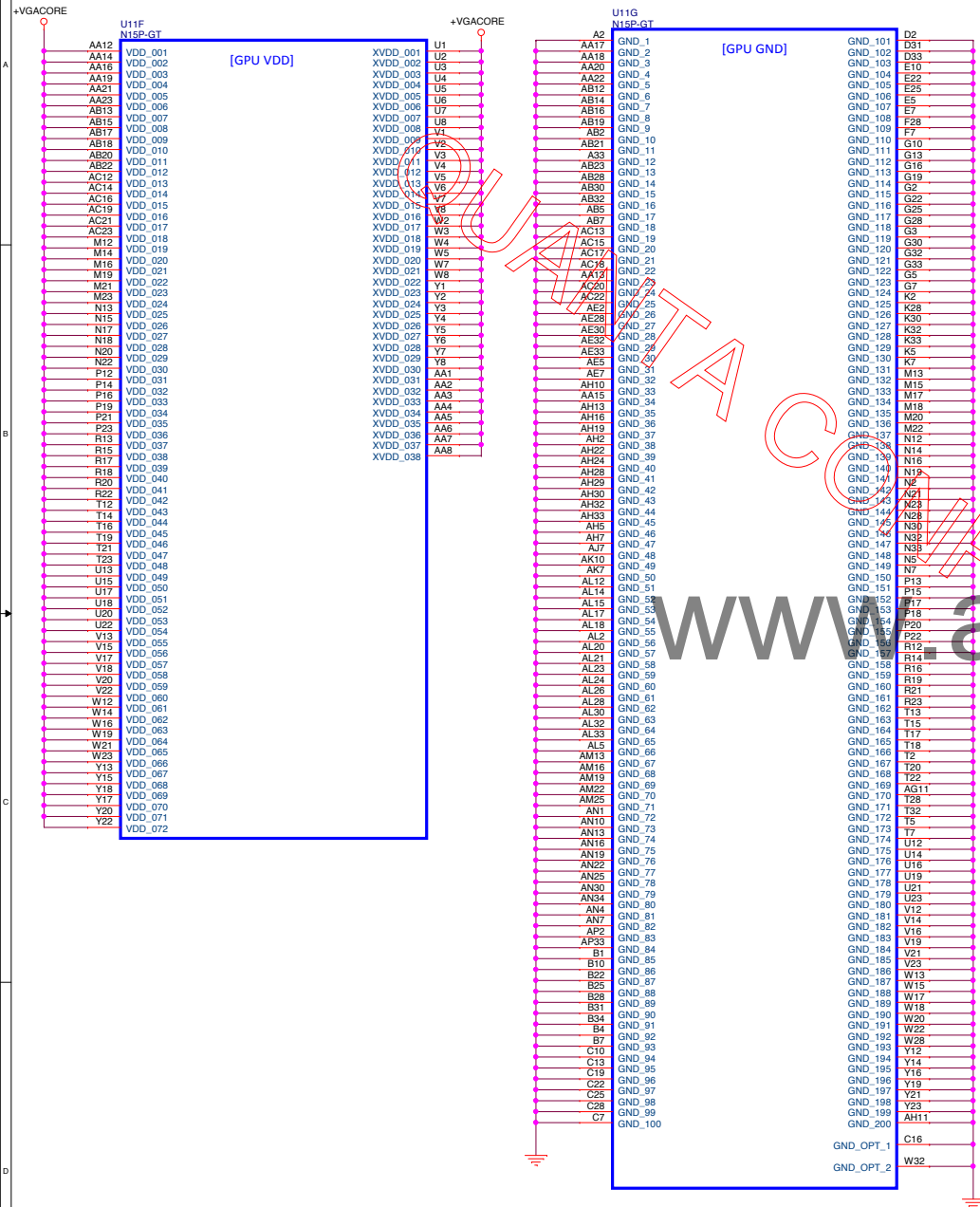
Resistor Values	Pull-Up to 3V3_MAIN	Pull-Down to GND
4.99 kΩ	1000	0000
10.0 kΩ	1001	0001
15.0 kΩ	1010	0010
20.0 kΩ	1011	0011
24.9 kΩ	1100	0100
30.1 kΩ	1101	0101
34.8 kΩ	1110	0110
45.3 kΩ	1111	0111

www.aitech1.ru

GPIO ASSIGNMENTS

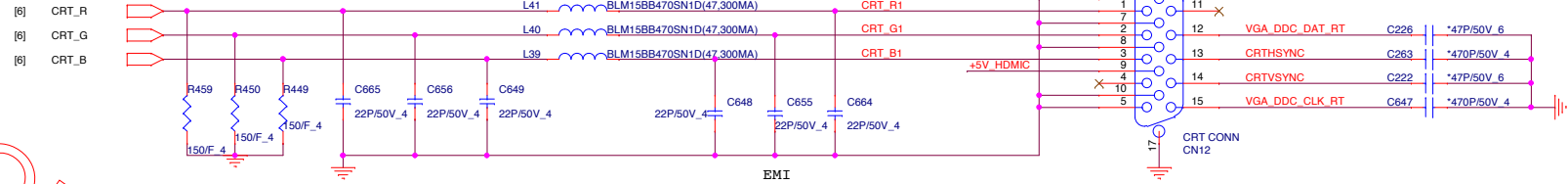
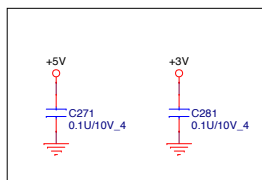
GPIO	GMT07/GMT08	GK208/GK107
GPIO 0	GC6_FB_EN	GPIO_FB_CLAMP
GPIO 1	MEM_VDD_CTL	MEM_VDD_CTL
GPIO 2	LCD_BL_PWM	LCD_BL_PWM
GPIO 3	LCD_PWR_EN	LCD_PWR_EN
GPIO 4	LCD_BL_EN	LCD_BL_EN
GPIO 5	GC6_PWR_EN	DEBUG SERVICE HEADER
GPIO 6	GPU_EVENT*	Remote Sensor Error Correction
GPIO 7	DEBUG SERVICE HEADER	3D STEREO
GPIO 8	SYS_PEX_RST_MON*	GPU OVERTEMP
GPIO 9	Remote Sensor Error Correction	GPU THERMAL ALERT/FAN_PWM
GPIO 10	MEM_VREF_CTL (N/A)	MEM_VREF_CTL
GPIO 11	NVDD_PWM_HD	NVDD_PWM_VID
GPIO 12	AC DETECT	AC DETECT
GPIO 13	NVDD_PSI	NVDD_PSI
GPIO 14	IFPD_HDP	N/C
GPIO 15	N/C	N/C
GPIO 16	FRAME LOCK	FRAME LOCK
GPIO 17	IFPD_HDP(DP)	IFPD_HDP(DP1/IM)
GPIO 18	IFPE_HDP(DP1/IM)	IFPE_HDP(DP1/IM)
GPIO 19	IFPF_HDP(DP1/IM)	IFPF_HDP(DP1/IM)
GPIO 20	GC6_MODE	N/A
GPIO 21	GPU_PEX_RST_HOLD*	N/A

VDD/XVDD : 25.72A

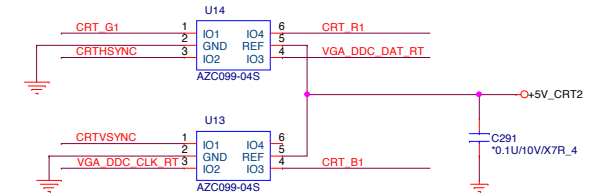


1

CRT PORT



ESD PROTECTION

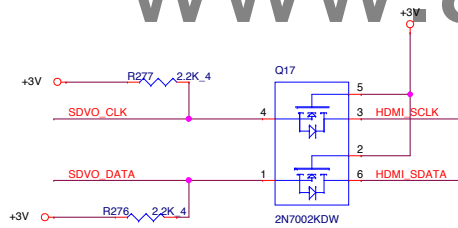


HDMI PORT

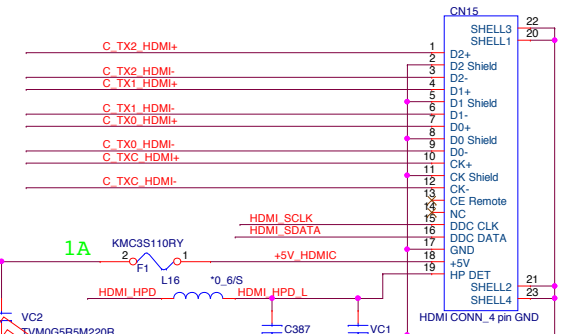
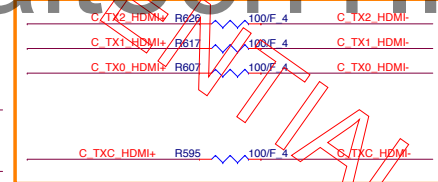
close to HDMI conn

Close to HDMI Connector

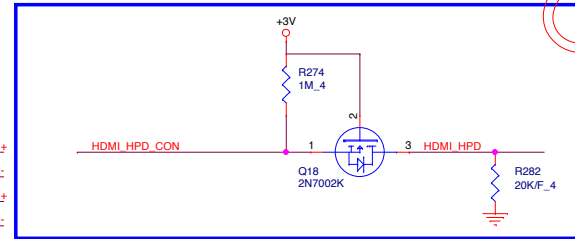
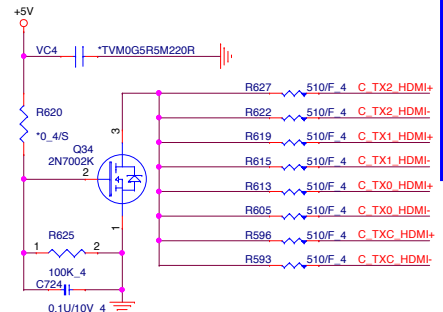
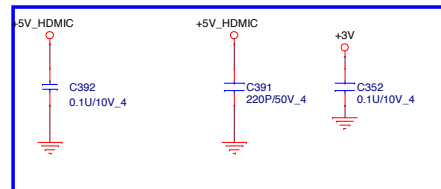
[2]	IN_CLK#	IN_CLK#	C698	0.1u/10V_4	C TXC HDMI+
[2]	IN_CLK	IN_CLK	C702	0.1u/10V_4	C TXC HDMI+
[2]	IN_D0#	IN_D0#	C708	0.1u/10V_4	C TX0 HDMI+
[2]	IN_D0	IN_D0	C709	0.1u/10V_4	C TX0 HDMI+
[2]	IN_D1#	IN_D1#	C713	0.1u/10V_4	C TX1 HDMI+
[2]	IN_D1	IN_D1	C714	0.1u/10V_4	C TX1 HDMI+
[2]	IN_D2#	IN_D2#	C716	0.1u/10V_4	C TX2 HDMI+
[2]	IN_D2	IN_D2	C721	0.1u/10V_4	C TX2 HDMI+



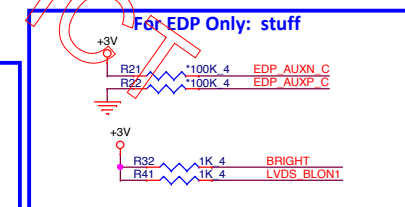
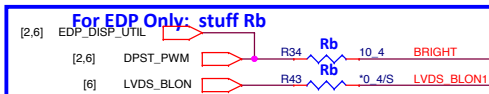
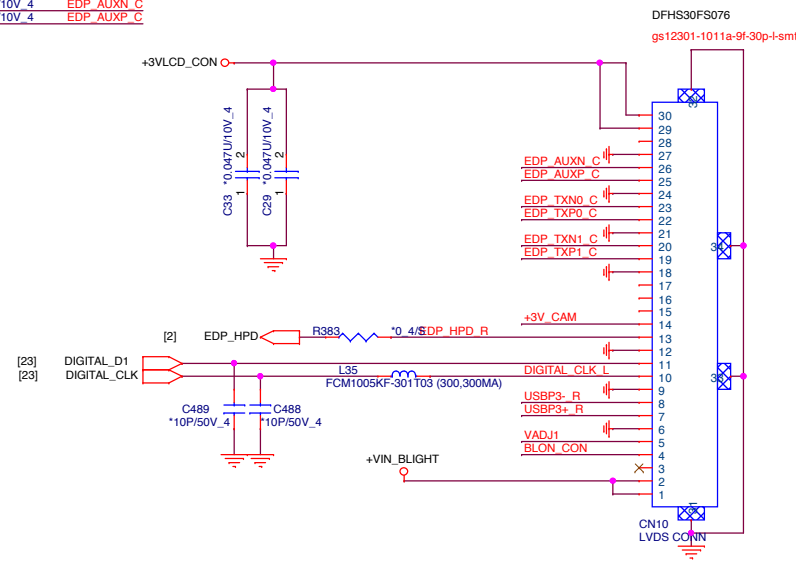
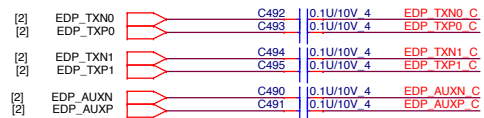
EMI request 0430@RNY Change EMI resistor to 100ohm

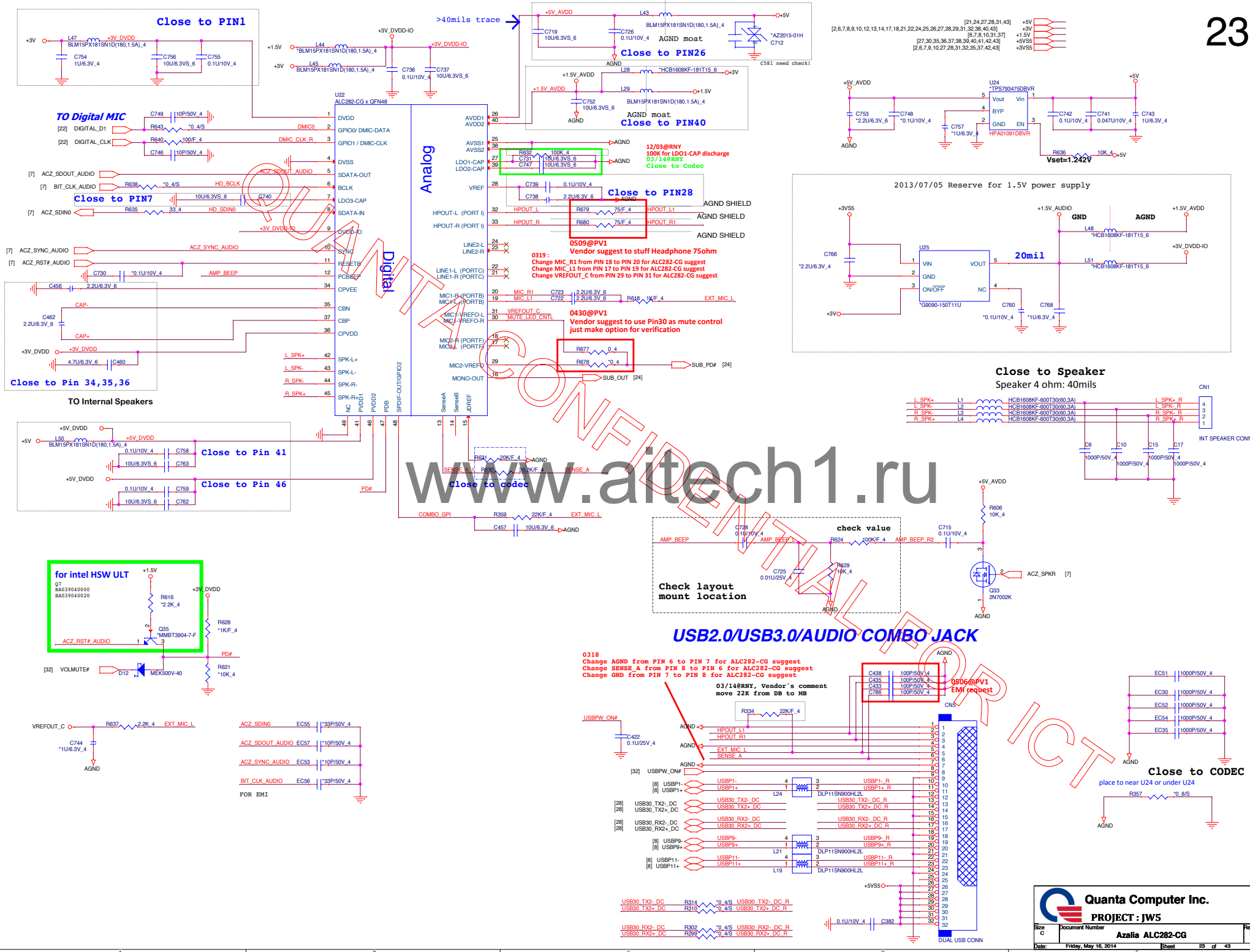


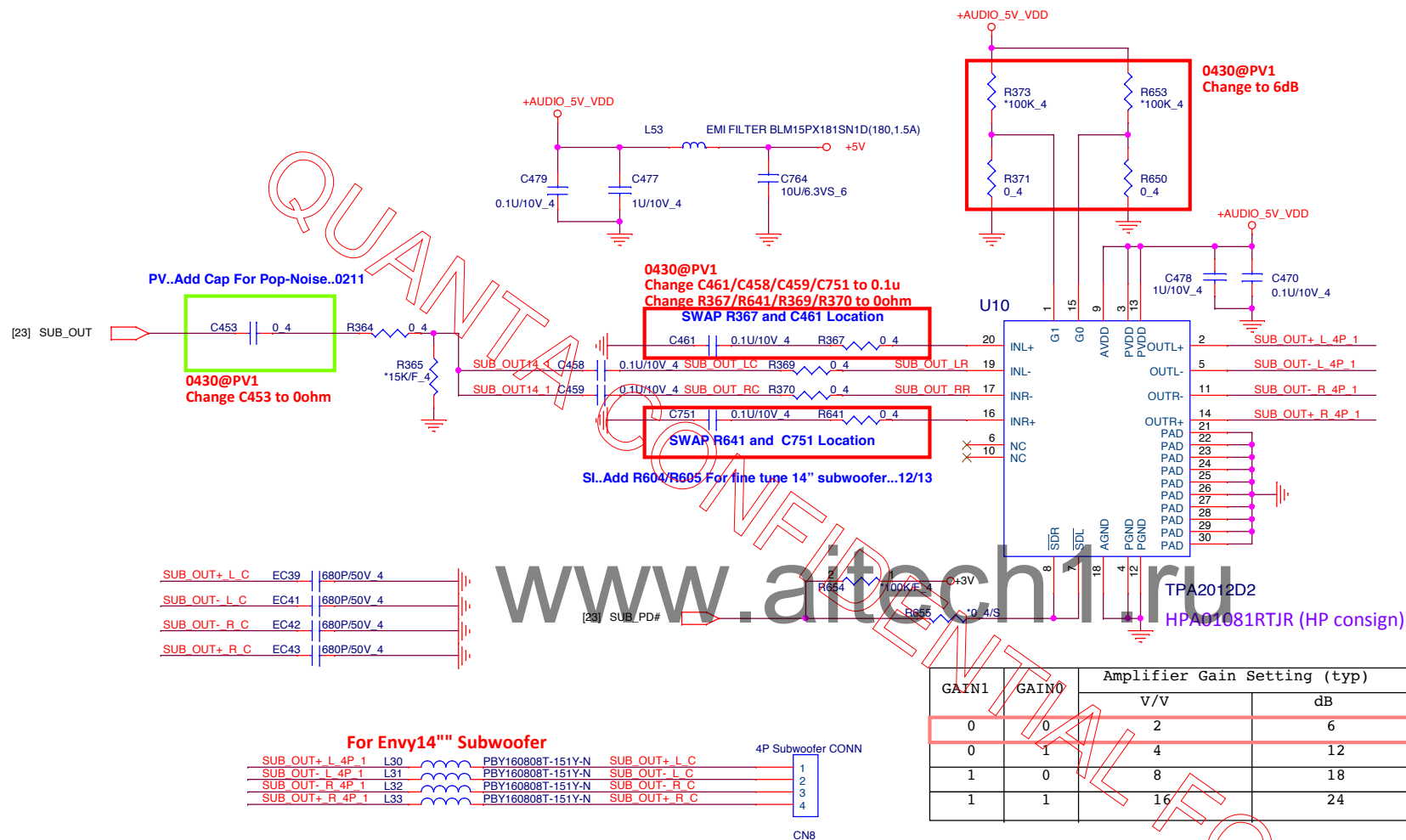
EMI request

+5V
+3V
+5VSS

22







[8] PCIE_CLKREQ_CR# PCIE_CLKREQ_CR# R670 0.4/S PCIE_CLKREQ_CR# R

[6,26,31,32] PCIE_WAKE# R668 0.4/S

Zdiff = 100 ohm

[8] CLK_PCIE_CRP
[8] CLK_PCIE_CRN
[8] PCIE_RXP3_CARD
[8] PCIE_RXN3_CARD

[2,8,14,26,31,32] PLTRS#

Please add 9 GND VIA connection with thermal PAD

RTS5227E-GRT

Close to chip pin

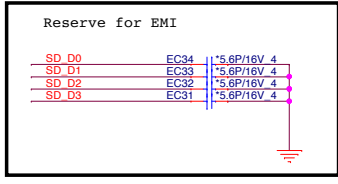
Close to chip pin

need close to Chip

CLOSE CONN

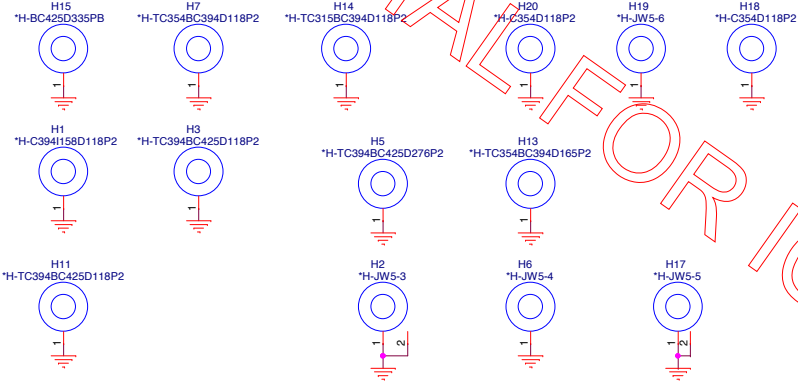
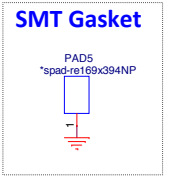
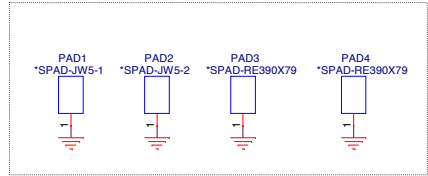
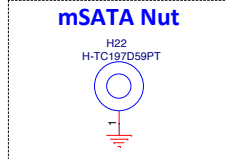
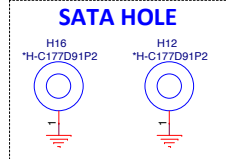
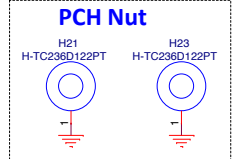
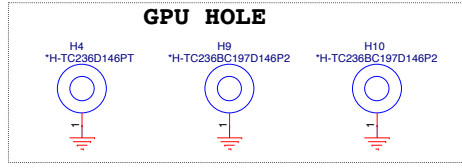
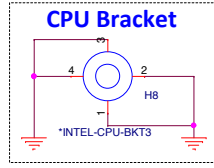
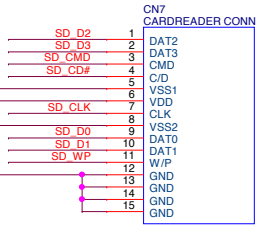
SD / MMC CARD READER



[2,6,7,8,9,10,12,13,14,17,18,21,22,23,24,26,27,28,29,31,32,36,40,43] +3V



SP1	SD D1	MS D1
SP2	SD D0	MS D0
SP3	SD CLK	MS D0
SP4	SD CMD	MS D2
SP5	SD D3	MS D3
SP6	SD D2	MS CLK
SP7	SD WP	MS BS

Share Pin

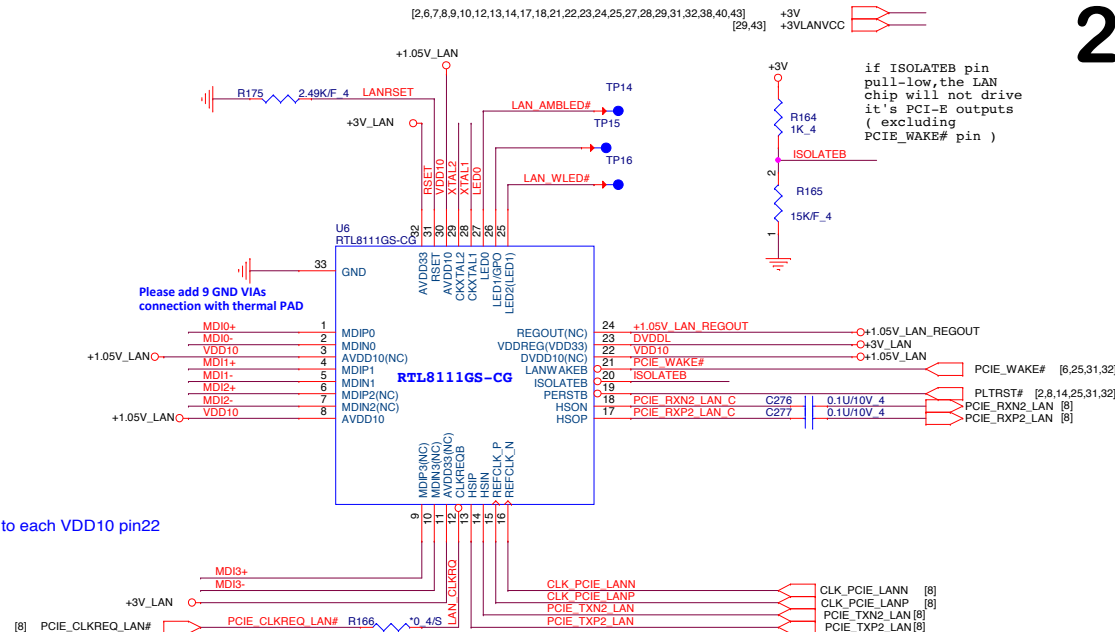


3]  

```

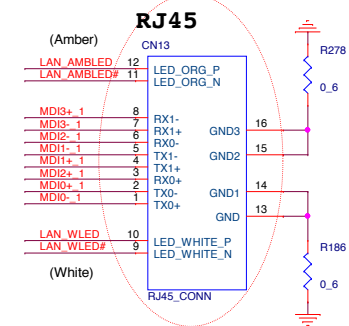
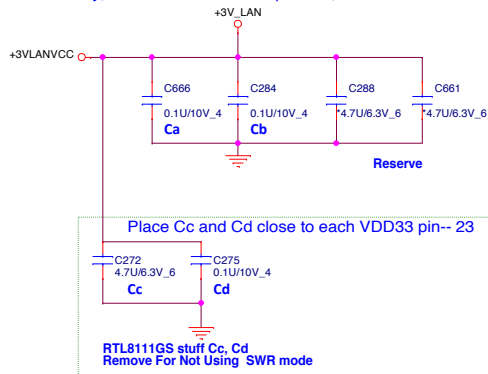
if ISOLATED pin
pull-low, the LAN
chip will not drive
it's PCI-E outputs
( excluding
PCI-E WAKE# pin )

```

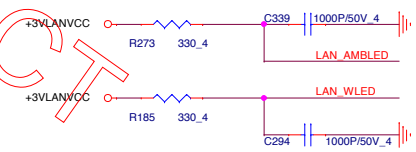
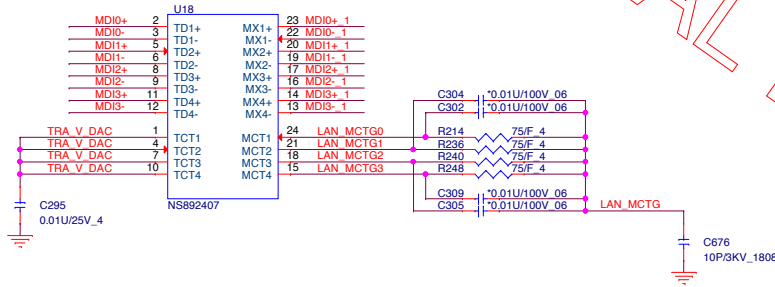


The schematic diagram illustrates the power and signal connections for the RTL8111GS-CG Ethernet controller. Key components and connections include:

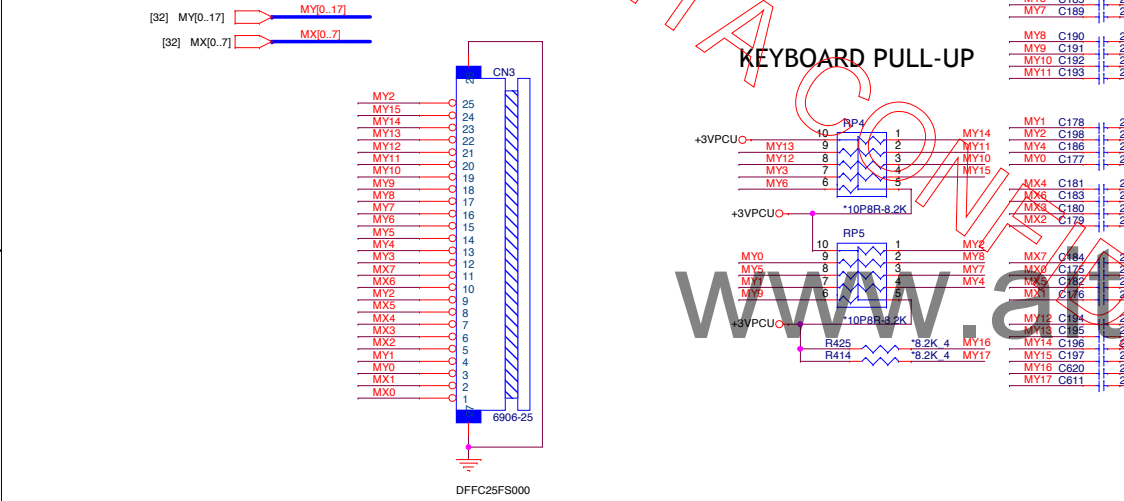
- Power Supply:** The circuit is powered by a +1.05V_LAN supply. A network of decoupling capacitors (Cc, Cd, Ce, Cf, Cg, Ch) is connected to the VDD10 pins (pins 3, 8, 22, 30) to ensure stable power. A separate +3V_LAN supply is connected to the MDI3+ pin (pin 16).
- Signal Connections:**
 - MDI0 pins (1-8):** MDI0+ (1), MDI0- (2), VDD10 (3), MDI1+ (4), MDI1- (5), MDI2+ (6), MDI2- (7), MDI2(NC) (8).
 - MDI3 pins (13-16):** MDI3+ (16), MDI3- (13), MDI3(NC) (14), MDI3(NC) (15).
 - LAN pins (17-24):** LAN_CLKREQ (17), LAN# (18), LAN_MCTG0 (19), LAN_MCTG1 (20), LAN_MCTG2 (21), LAN_MCTG3 (22), LAN_TXN2 (23), LAN_TXP2 (24).
 - Other pins:** REGOUT(NC) (25), VDDREG(VDD33) (26), DVDD10(NC) (27), LANWAKEB (28), ISOLATEB (29), PERS1B (30), HSON (31), HSOP (32).
- Decoupling Capacitors:** Cc (0.1u/10V_4), Cd (0.1u/10V_4), Ce (0.1u/10V_4), Cf (0.1u/10V_4), Cg (0.1u/6.3V_4), Ch (0.1u/10V_4), C282 (0.1u/10V_4), C288 (4.7u/6.3V_6), C661 (4.7u/6.3V_6), C295 (0.01u/25V_4), C676 (10p/3KV_1808).
- Resistor Network:** A resistor network (R214, R236, R240, R248) is used to divide the +3V_LAN supply to provide a 75F 4 signal to the LAN_MCTG pins.



0304@RNY
follow JW2, 確認pin define and PN



KEYBOARD Con.



0430@PV1
add KB light circuit

[32] KB_LED_EN

+VIN

R673
1M_4

Q36
AO3404

+5V

R674
2M_4

Q37
2N7002

+5V_LED_KBLIGHT

C784
0.1U/10V_4

C785
0.1U/10V_4

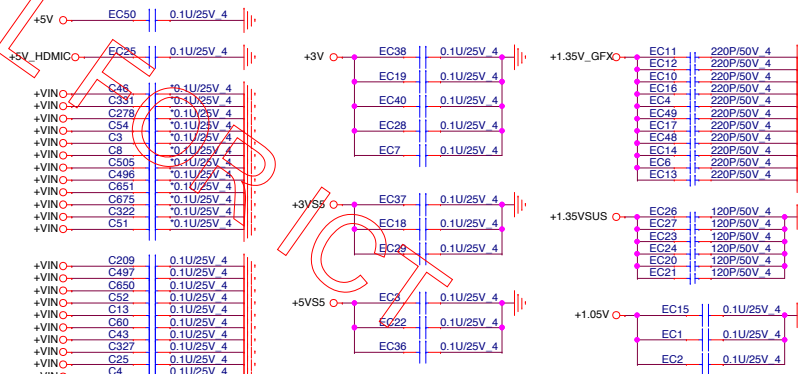
CN18

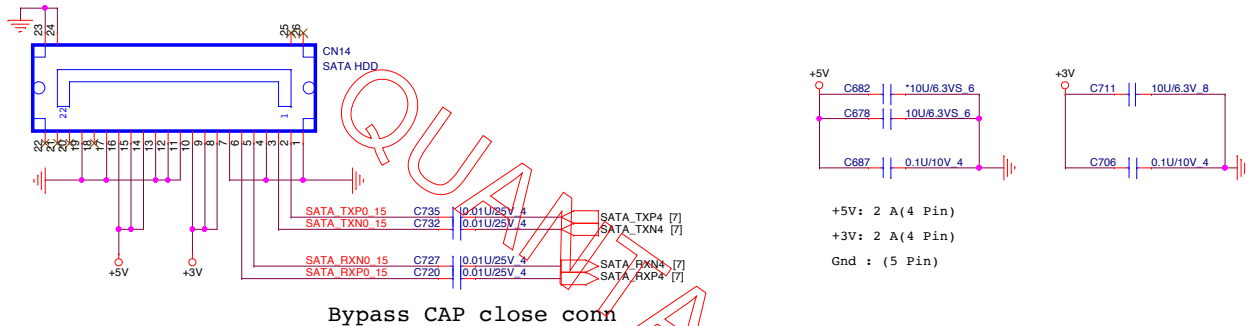
KB_LIGHT_CONN_15

[2,6,7,8,9,10,12,13,14,17,18,21,22,23,24,25,26,28,29,31,32,36,40,43] +3V

[21,23,24,28,31,43] +5V

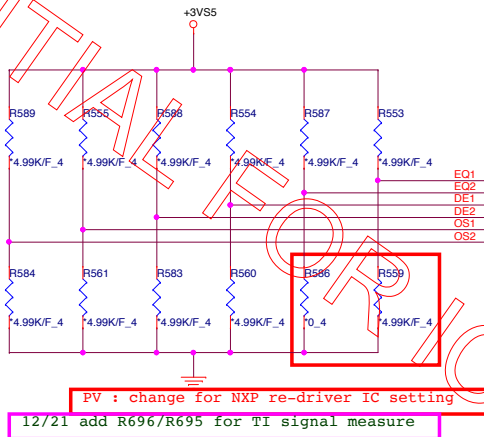
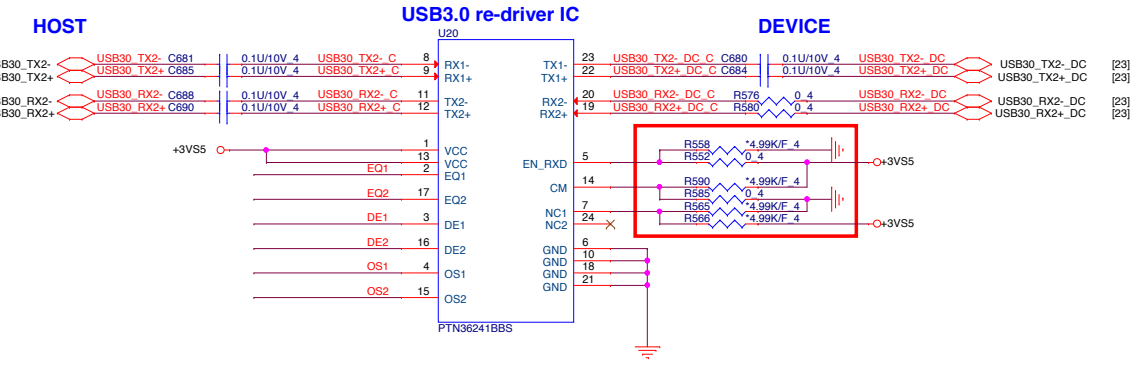
[4,7,29,31,32,34,35] +3VPCU



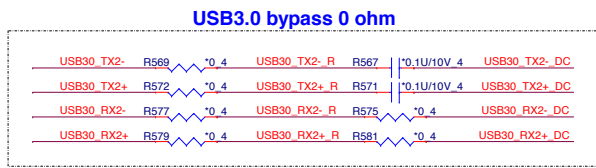


USB3.0
USB3.0 Re-driver IC

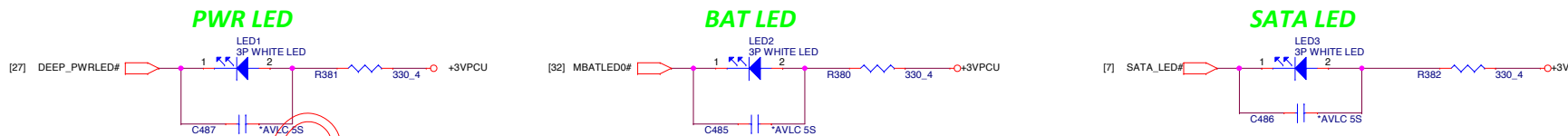
www.aitech1.ru



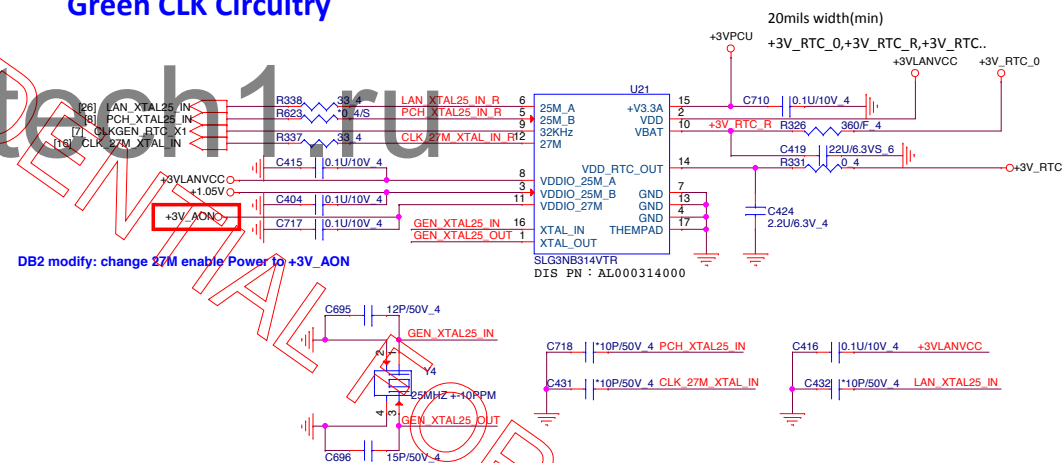
OSx		Transition Bit Amplitude	
NC(default)		1000	
0		870	
1		1085	
EQx		Equalization dB	
NC(default)		0	
0		7	
1		15	
DEx	OSx=NC	OSx=0	OSx=1
NC	-3.5dB	-2.2dB	-4.4dB
0	-6.0dB	-5.2dB	-6.0dB
1	-8.5dB	-8.9dB	-7.6dB
EN_RXD		DEVICE FUNCTION	
1(default)		Normal operating mode	
0		Sleep mode	
CM		DEVICE FUNCTION	
0(default)		Normal operating mode	
1		Compliance mode	



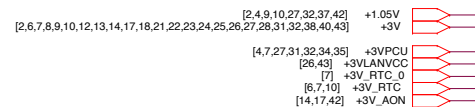
LED Status



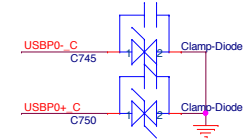
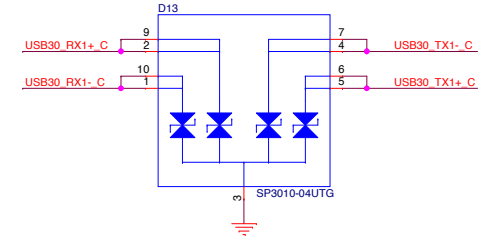
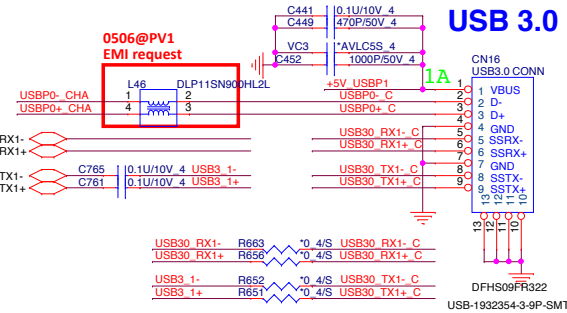
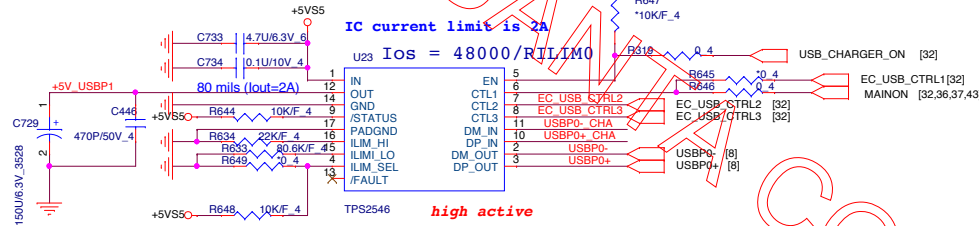
Green CLK Circuitry



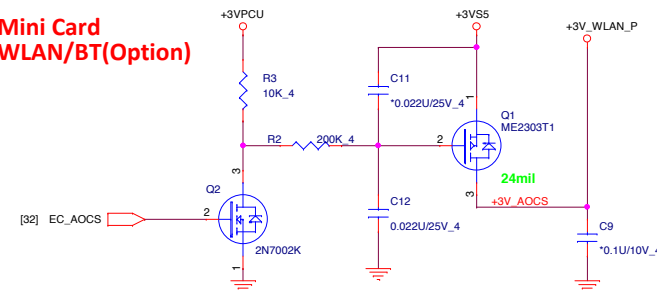
DB2 modify: change 27M enable Power to +3V AON



for Envy SKU stuff



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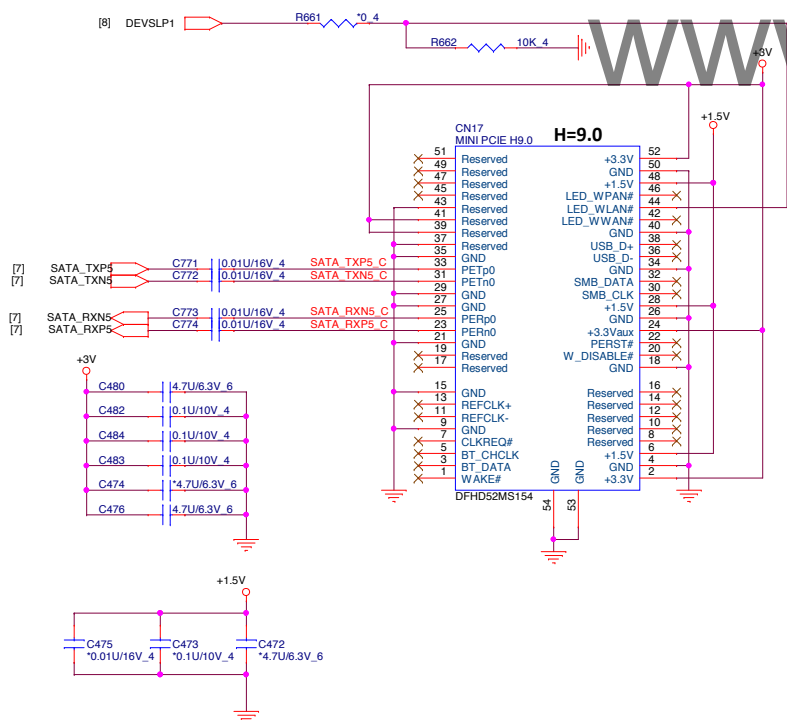
Support Wake Function(Reserve)

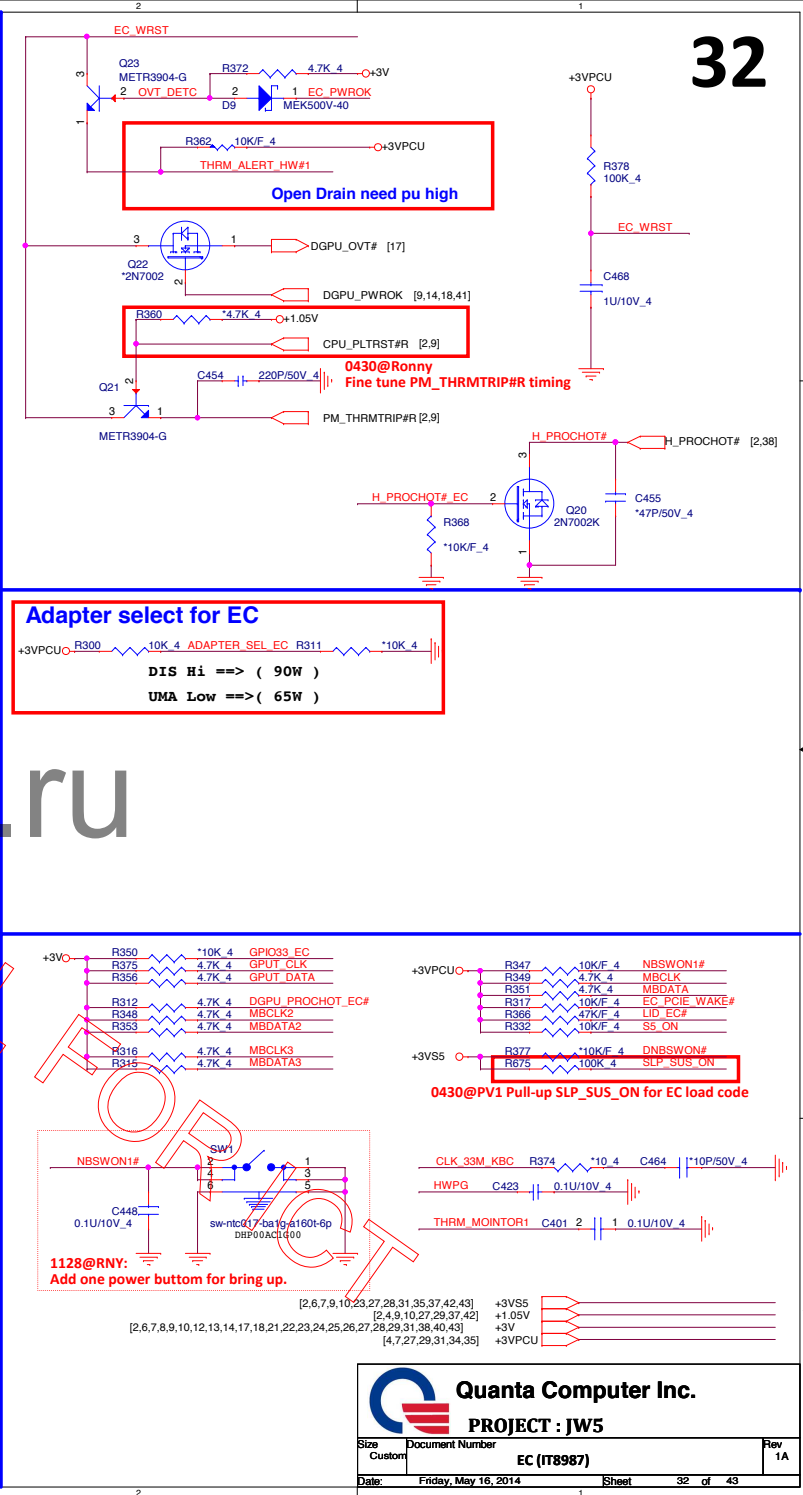
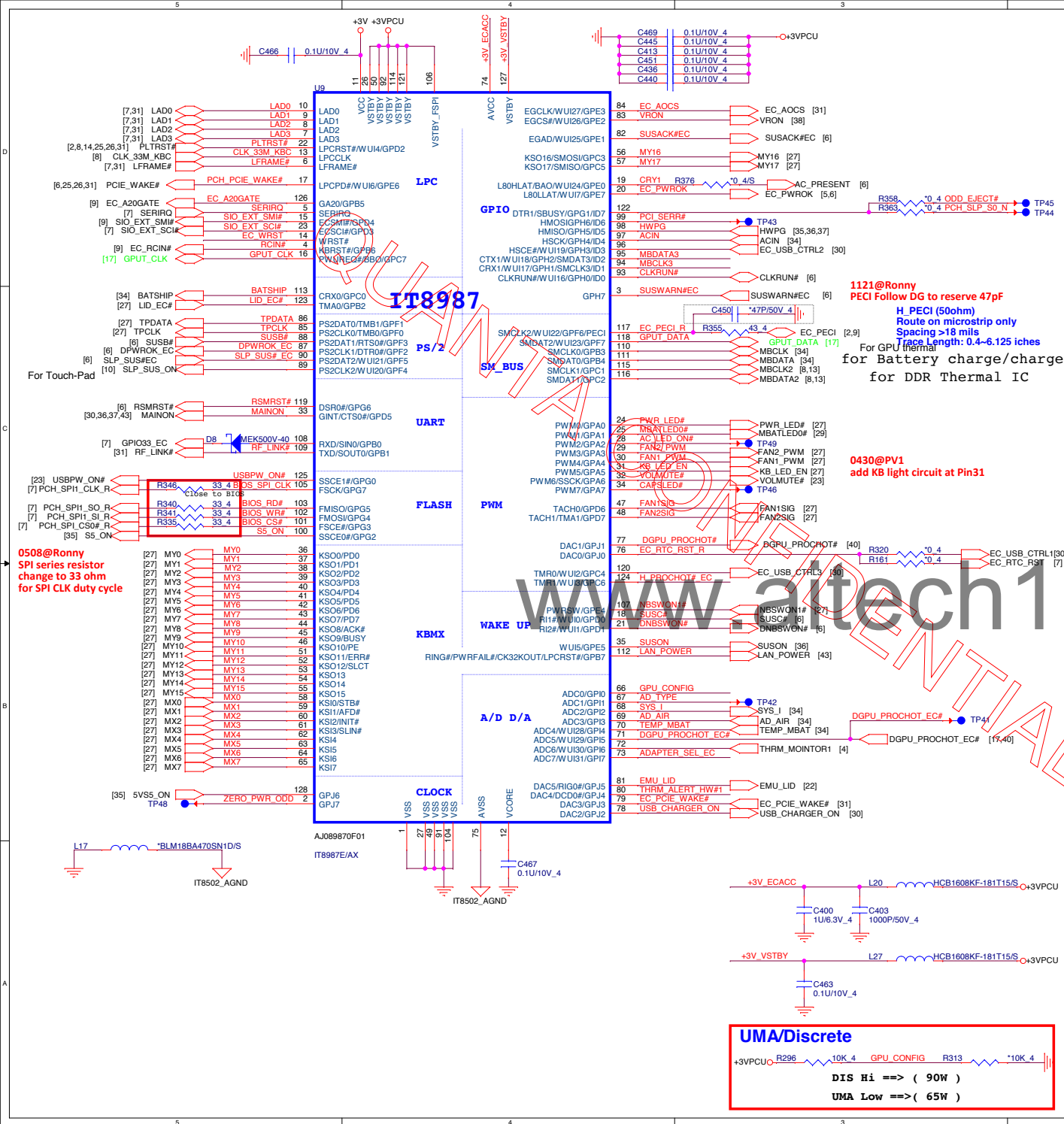
The diagram illustrates the support wake function circuit. It features two identical components, DRC5144E0L, each with three pins. The top component's pin 2 is connected to +3V_WLAN_P, pin 1 to MINICAR_PME#, and pin 3 to PCIE_WAKE# [6,25,26,32]. The bottom component's pin 2 is also connected to +3V_WLAN_P, pin 1 to MINICAR_PME#, and pin 3 to EC_PCIE_WAKE# [32]. A resistor R55 (10K/F_4) is connected between the MINICAR_PME# line and the PCIE_WAKE# line of the bottom component.

```

9/4 Intel COMBO card control circuit
1.add R1001,R1002,Q1001
2.add net name"INT BT COMBO EN#" -> "INT BT OFF#"


```





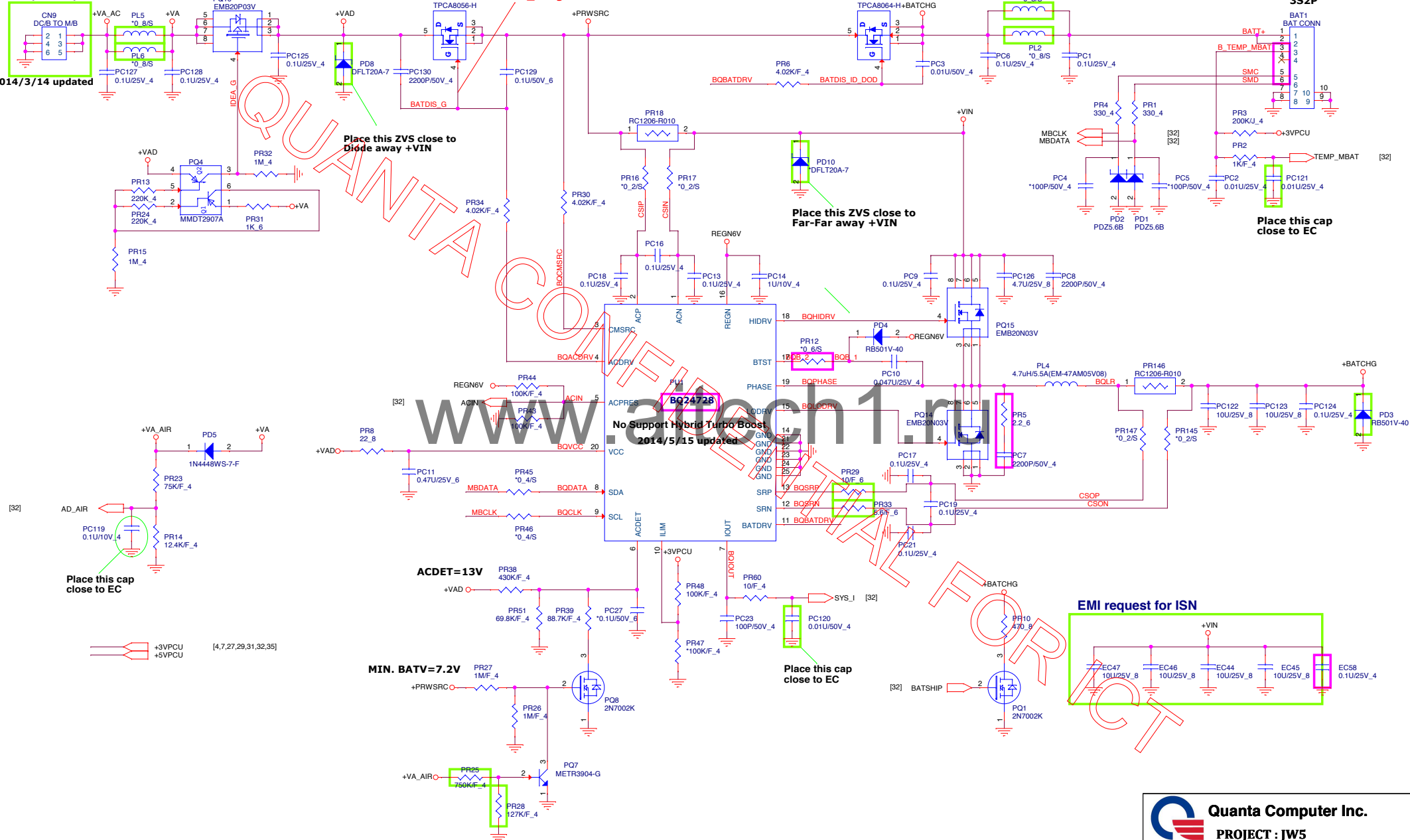
QUANTA CONFIDENTIAL FOR ICT

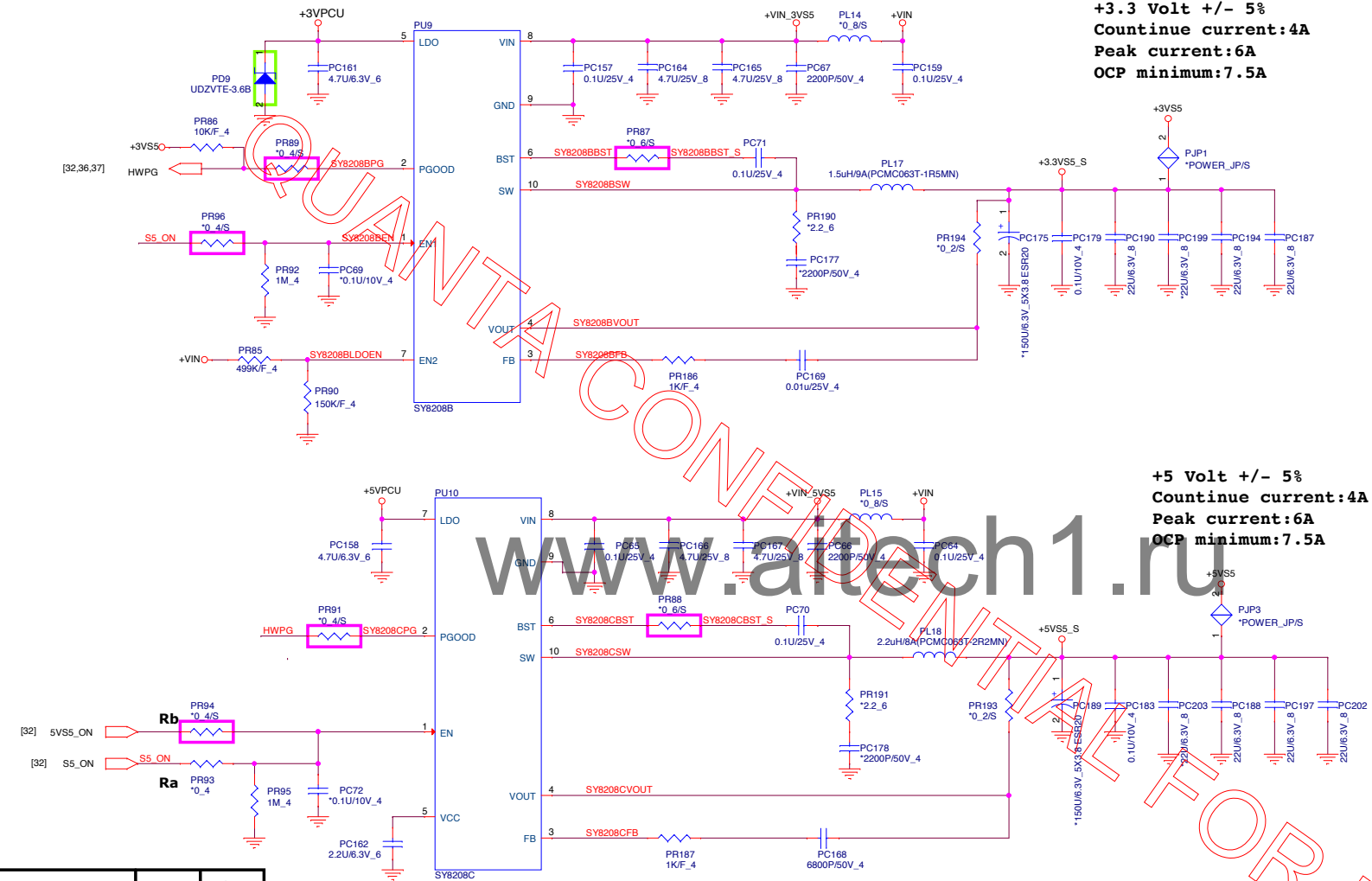
www.aitech1.ru

		Quanta Computer Inc.	
<Title>		PROJECT : JW5	
Size A	Document Number <Doc>		Rev 1A
Date:	Friday, May 16, 2014	Sheet	33 of 43

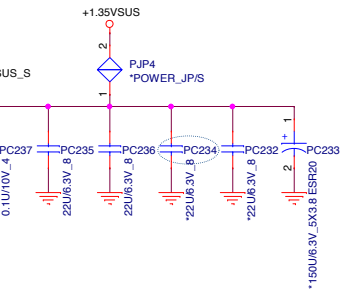
DC JACK
19V/120W/6.5A

2014/3/14 updated

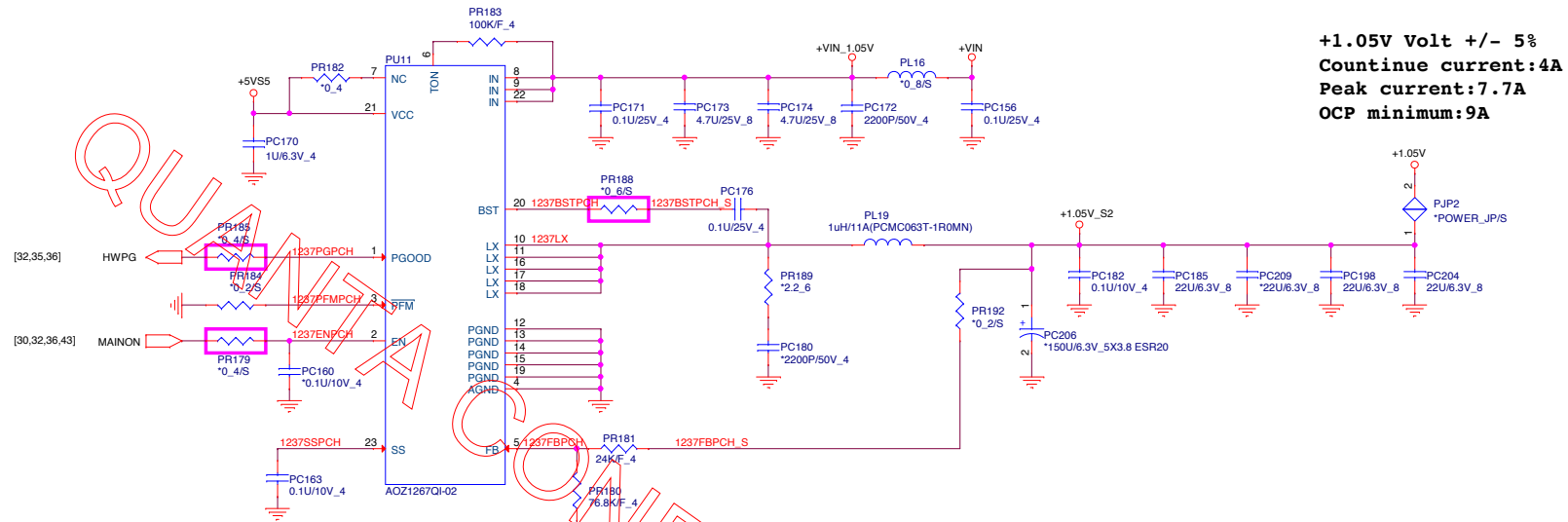




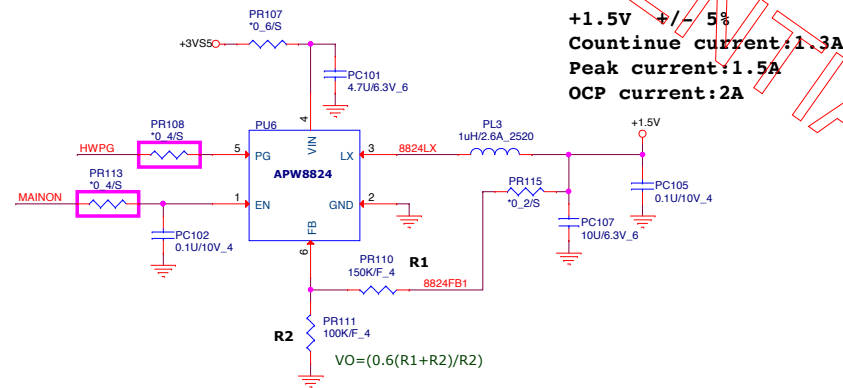
USB Charge Support	Ra	Rb
VINE (No support)	Stuff	NA
ENVY (Support)	NA	Stuff



+1.35VSUS [2,4,12,13,27]

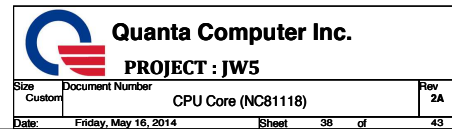


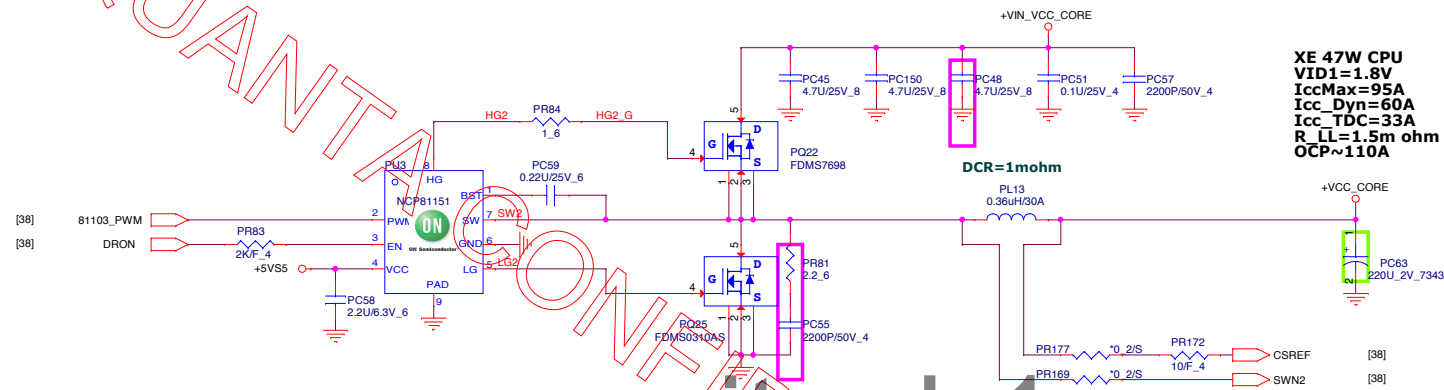
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+VIN [22,27,34,35,36,38,40,41,42,43]
+3VS5 [2,6,7,9,10,23,27,28,31,32,35,42,43]
+5VS5 [23,27,30,35,36,38,39,40,41,42,43]

CPU	Rd	P/N
37W	???	???
47W	75K	CS37502FB12





XE 47W CPU
VID1=1.8V
IccMax=95A
Icc_Dyn=60A
Icc_TDC=33A
R_LL=1.5m ohm
OCP~110A

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+VCC_CORE [4,38]

